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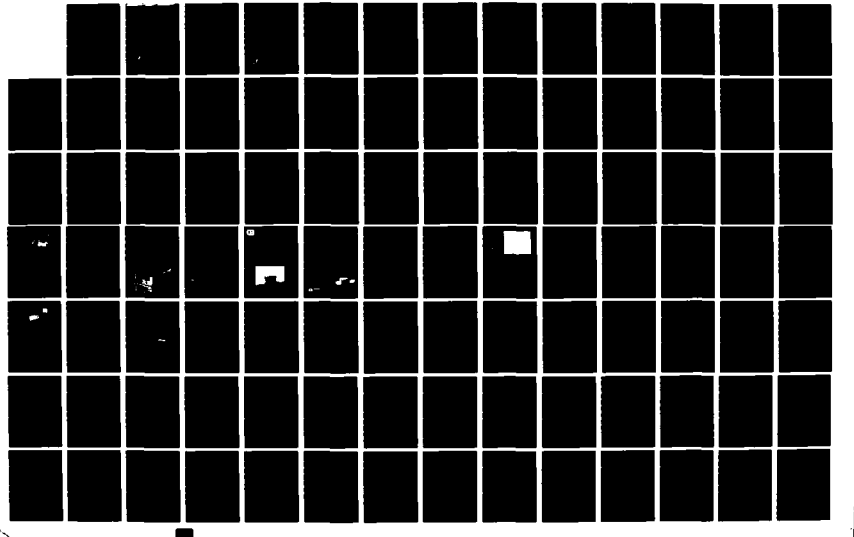

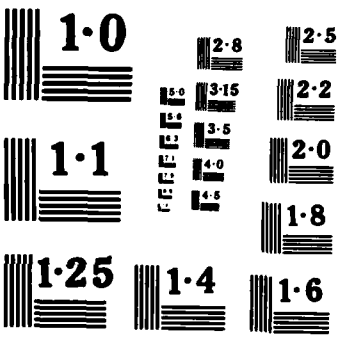

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NSWC TR 85-133

MASS MEMORY STORAGE DEVICES FOR AN/SLQ-32(V)

By L. C. TRIOLA

ELECTRONICS SYSTEMS DEPARTMENT

1 JUNE 1985

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AN/SLQ-32(V) Suite	Magnetic Hard Disk	Bernoulli Disk Drive
AN/UYK-19 Computer	Optical Disk	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This technical report documents the investigation of mass memory storage devices for use with AN/SLQ-32(V) electronic warfare suites. The device is to be incorporated into the AN/SLQ-32(V) systems in order to reduce the program loading time and the operator actions required for the load. The report includes specific details on five types of mass memory storage devices: magnetic hard disks, optical (laser) disks, magnetic bubble memory, dynamic RAM with battery backup, and Bernoulli disk drives.

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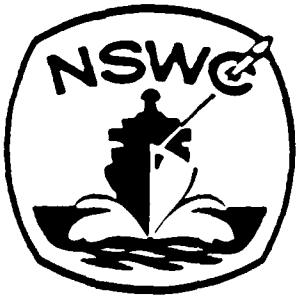

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EXECUTIVE SUMMARY

The purpose of the investigation of mass memory storage devices was to find a way to improve the speed of loading the AN/SLQ-32(V) computer programs. If the present system is not augmented for future software expansion, the time to load a complete set of tactical programs and libraries into the AN/UYK-19 computer, the RP-16 microprocessor, and other peripheral processors (e.g., ADLS and Band 1) will be five minutes or more. This time span is unacceptable for combat situations.

The approach of the investigation included three stages:

1. Evaluation of the requirements for software storage

2. Consideration of all options which might meet these requirements

3. Detailed investigation of the most feasible options

An evaluation of the requirements for data storage revealed that the storage capacity would have to be a minimum of 700 kilobytes for the tactical programs and libraries alone or 3 megabytes if the diagnostic software also resides in the memory device. Data access and transfer rates should be such that the entire tactical software set could be loaded within ten seconds or less.

Consideration of all options which might meet these requirements included modification of the present tape system. It was determined that neither modification of the present tape drive nor obtaining a new tape drive system would sufficiently improve software load time. Ten different types of mass storage systems were also considered: magnetic hard disk, floppy disk, optical disk, magnetic bubble memory, EPROM, EEPROM, nonvolatile RAM, magnetic core, static or dynamic RAM with battery backup, and Bernoulli disk drives. Five were eliminated from consideration because of functional problems or expense.

The five remaining types (hard disk, optical disk, bubble memory, RAM with battery backup, and Bernoulli disk drive) were investigated in detail. No type of device was found to be ideal. Each had both advantages and disadvantages, which are described in this report.

Engineering and programming considerations for interfacing a new storage device with the present AN/SLQ-32(V) system are also discussed. The device will require a direct connection to the AN/UYK-19 computer, either by the I/O bus or by direct memory addressing. The device will have to be mounted close to the AN/UYK-19 in already crowded equipment rooms. Software for the computer and the peripheral processors, including the RP-16, will have to be

rewritten to accommodate the new concept of loading directly from the mass storage device. At the same time the current method of program loading must be retained for the purposes of program backup and software delivery.

This report recommends prototyping the most promising devices if sufficient time and funds are available. These prototypes should be tested to prove survivability and performance aboard ships operating under extreme environmental conditions. The production contract should be submitted for competitive bids to ensure the best cost/performance ratio.

FOREWORD

This work has been performed under a NAVELEX PDE-107 funded task to investigate mass memory storage devices for the purpose of improving AN/SLQ-32(V) program load time. The requirements for such a device are described in Chapter 2. Present system modification and hardware options which would decrease load time are discussed in Chapters 3 and 4. The most feasible hardware options are described in detail in Chapter 4. Engineering and programming considerations, conclusions, and recommendations are included in the last three chapters.

This report, which has been reviewed by the head and members of the System Engineering Group (F2450), by the head of the Electronic Countermeasures (ECM) Branch (F24), and by the head of the Electronic Warfare Division (F20), is hereby released for publication.

Approved by:

R. T. RYLAND, Jr., Head
Electronics Systems Department

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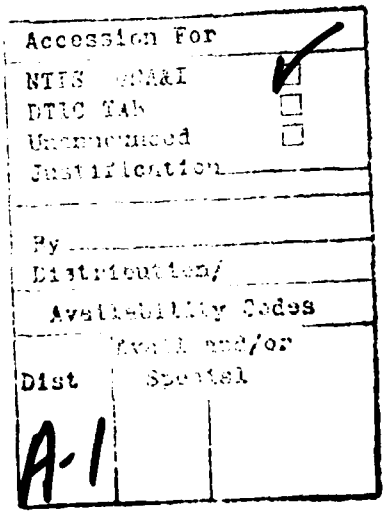

CONTENTS

ILLUSTRATIONS

TABLES

CHAPTER 1

INTRODUCTION

AN/SLQ-32(V) electronic warfare (EW) systems are installed aboard ships in the U.S. Naval fleet to detect, analyze, and identify radio frequency emitters. They also recommend or activate electronic countermeasures against emitters identified as hostile (e.g., missiles). For the system to become operational, the system software must be loaded into computer memory from the 4-track magnetic tape cartridges (MTCs) on which the programs are stored.

Program load begins when the operator inserts the operational program MTC and presses the Program Load button on the Display and Control Console (DCC). Loading current versions of the operational program requires over one minute; and loading future, expanded versions of the program will require even more time. If an operator wishes to use a threat summary library geographically tailored to that ship's global region, the library must be loaded from a separate MTC after operational program load is complete. With future software expansion the entire loading process could require five minutes or more. This time span is unacceptable for combat situations since a ship could be targeted and destroyed before the AN/SLQ-32(V) system became operational.

NAVELEX PDE-107 tasked the Electronic Countermeasures (ECM) Systems branch (F24) at the Naval Surface Weapons Center (NSWC) in Dahlgren, VA, to investigate the addition of a mass memory storage device to the AN/SLQ-32(V) system in order to reduce the time required for program load. This report summarizes the investigation. It includes the requirements for such a mass storage device, the options available, and the engineering considerations for implementing the device in the AN/SLQ-32(V) system.

CHAPTER 2

REQUIREMENTS

Any mass memory storage device incorporated into the AN/SLQ-32(V) system must meet certain minimal requirements in its storage capacity and in its speed of data access and transfer. Chapter 2 describes these requirements and other considerations.

STORAGE CAPACITY

An auxiliary mass storage device should be capable of storing all present and future AN/SLQ-32(V) operational and diagnostic programs and data bases. Present software includes the following:

1. Operational Program. The operational (tactical) program, which resides in AN/UYK-19 memory, contains data bases and decision-making processes to identify radar emitters, to inform the operator of threat and system statuses, and to command the system hardware to activate countermeasures.

2. RP-16 Program. The RP-16 program is used in conjunction with the operational program to enable the operator to communicate through the DCC to the AN/UYK-19.

3. CP-32 Program. The CP-32 program, which resides in the RP-16, performs debug functions.

4. System Diagnostic Tests. The System Diagnostic Test (SDT) software is used to detect and isolate hardware faults.

5. Threat Libraries. Independent main and on-line libraries are data bases of radar parameters used by the tactical software.

Future computer programs, which will reside in peripheral processors, include the Automated Decoy Launching System (ADLS) and Band 1.

As shown in Table 1, which lists the storage requirements for present and future programs, the total storage capacity of an auxiliary mass storage device would have to be at least 3 megabytes (1.5 megawords). This capacity could be reduced if SDT software were separately stored on tape. The slower load time resulting from the separate storage would be inconvenient but not combat critical.

TABLE 1. AN/SLQ-32(V) PROGRAMS AND DATA FILES

PROGRAM	16-BIT WORD LENGTH
OPERATIONAL	192 K
RP-16/CP-32	4 to 16 K
MAIN LIBRARY/EBASE	6.4 K 7.2 K (CDS)
ON-LINE LIBRARY	3 K each
SYSTEM DIAGNOSTIC TEST	750 K
FUTURE PROGRAMS	
ADLS	? (64 K - Not Completed)
BAND 1	20 to 32 K (Not Completed)

DATA ACCESS/TRANSFER

An auxiliary mass storage device for the AN/SLQ-32(V) system must be capable of accessing and transferring data from all current and future software within the shortest time span possible, certainly within ten seconds. In .der to obtain this rapid loading time, the new mass storage device would require an access (to beginning of information file) rate in milliseconds and a transfer (from device to device) rate of at least one megabit (125 kilobytes) per second.

As shown in Figure 1, the current computer/tape drive interface occurs within the DCC. When the operator presses the Program Load button, the RP-16 microprocessor firmware transfers data into the RP-16 random access memory (RAM). The AN/UYK-19 computer is loaded via the RP-16 program and the interface programmable read only memory (PROM) card.

Data access and transfer with a mass storage device would require the configuration shown in Figure 2. The AN/SLQ-32(V) system would have to be modified to permit direct communication between the AN/UYK-19 computer and the mass storage device for quick load of the peripheral processors and the AN/UYK-19 itself. Chapter 5 provides further details of the necessary configuration changes.

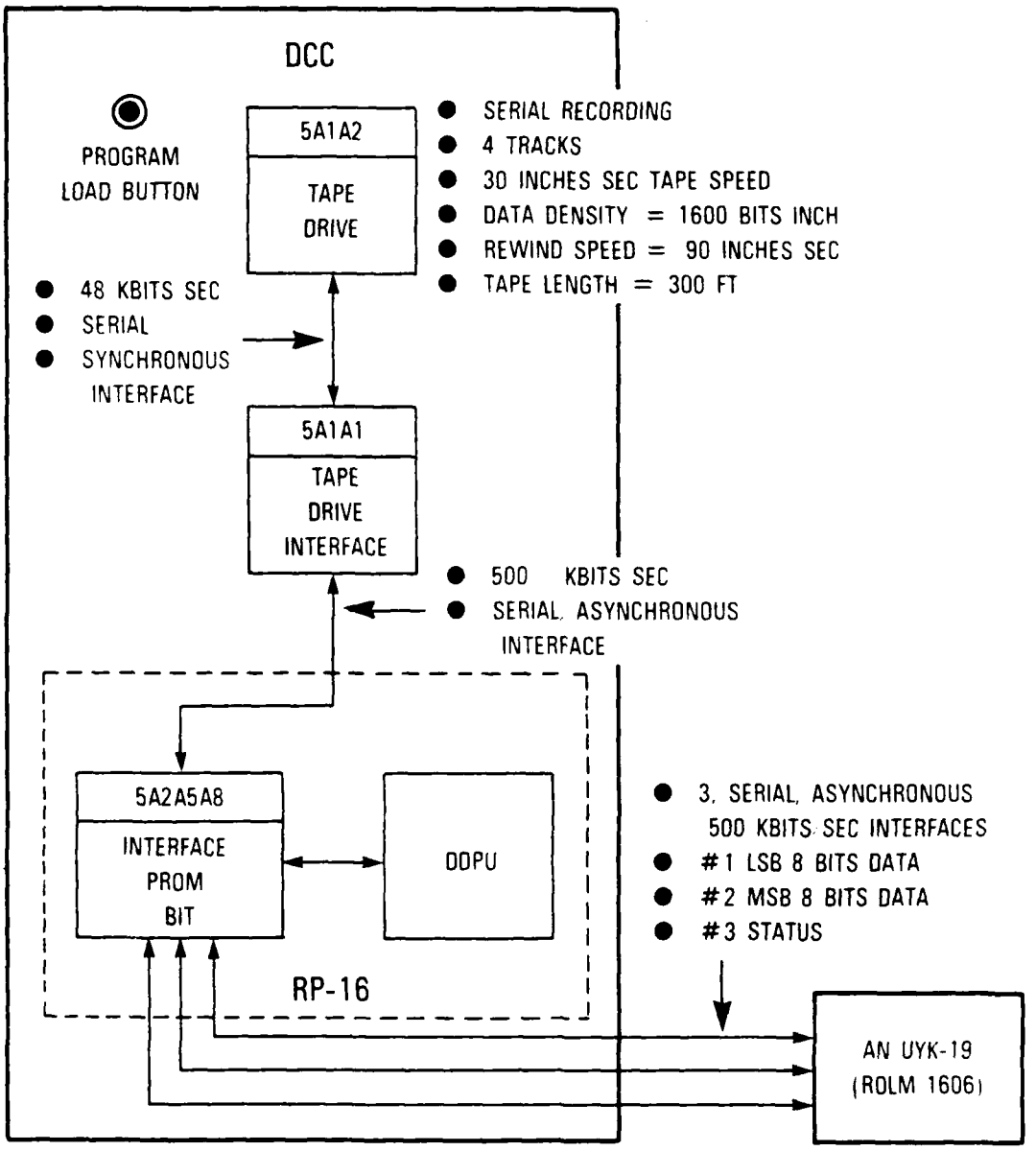

FIGURE 1. PRESENT AN/SLQ-32(V) TAPE DRIVE/COMPUTER INTERFACE

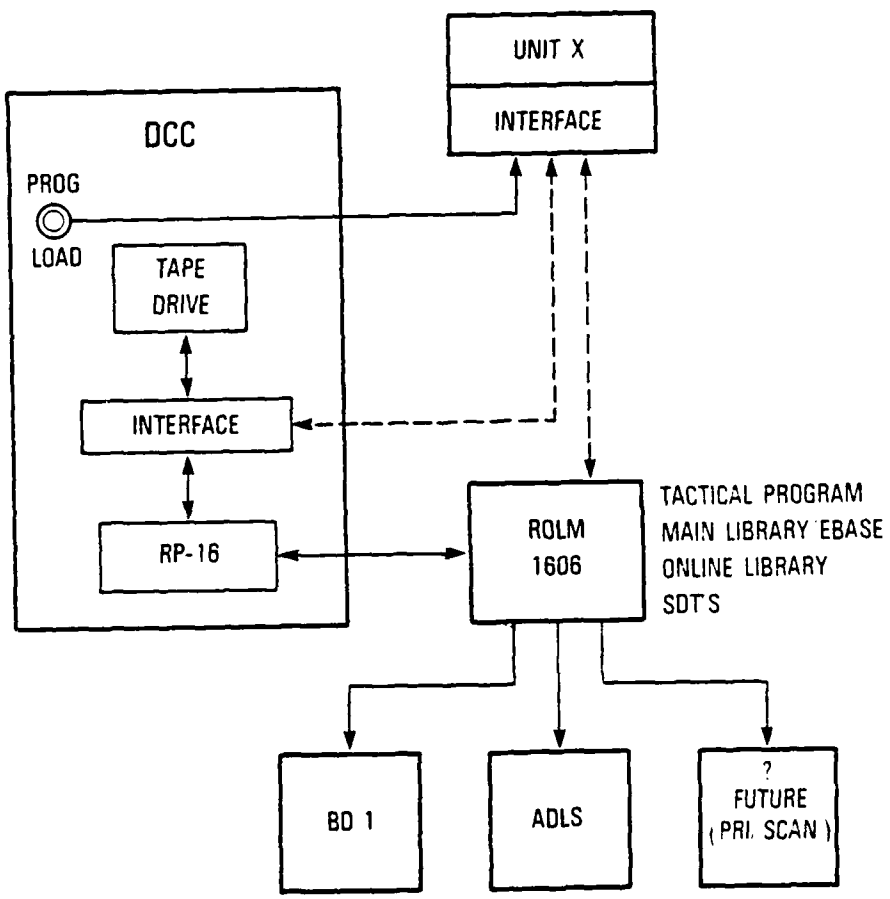

FIGURE 2. AN/SLQ-32(V) COMPUTER INTERFACES WITH PROPOSED MASS STORAGE DEVICE AND PERIPHERAL PROCESSORS

OTHER CONSIDERATIONS

Other considerations in the selection of a mass storage system for AN/SLQ-32(V) include reliability, ease of interface, physical size and mounting, conformance to military specifications, and cost.

CHAPTER 3

MODIFICATION OF PRESENT SYSTEM

NSWC personnel considered several options in its investigation of ways to reduce software load time. The first option was a modification of the present AN/SLQ-32(V) system.

Current program load involves the following steps (also see Appendix B):

1. Operator loads tactical program MTC into DCC tape transport unit.
2. Operator presses Program Load button.
3. MTC loads AN/UYK-19 and RP-16 memories at a maximum rate of 48,000 digital bits of information per second.*
4. Tape transport automatically rewinds MTC to beginning of tape.
5. Operator removes tactical program MTC.
6. Operator may opt to load separate geotailored threat libraries. (The operator who chooses a separate loadable library must follow further load instructions cued on the DCC CRT screen.)

The speed of data transfer in steps 3 and 6 could be improved through a modification of the present system. Current tactical software is stored on one half of a single track of the MTC at a storage density of 1,600 bits per inch. Two changes could increase the data transfer rate from 48,000 to 768,000 bits per second. First, a new tape drive could quadruple the tape's storage density, increasing it from 1,600 to 6,400 bits per inch. Second, data could be stored in parallel across all four tracks of the tape. These changes would require both a new, faster interface to allow the faster transfer of data bits and substantial software modification. Future computer load time might be reduced to one minute; however, the tape spooling and rewinding time and the operator's tape handling time are inherent to the system and could not be eliminated. Because modifying the present system as described would require substantial software modification for the parallel track storage and would still not reduce the load time sufficiently, it is not a good memory expansion option.

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* Actual testing by F24 personnel at NSWC has determined that loading the AN/UYK-19 and the RP-16 with the current C6R1-11 program (~140K words) requires 70 seconds.

CHAPTER 4

HARDWARE OPTIONS

Ten different types of mass memory storage hardware options were considered for the AN/SLQ-32(V) system. Pertinent characteristics of high memory capacity options (3+ megabytes) are presented in Table 2. Characteristics of low memory capacity options are presented in Table 3. None of the low memory capacity options are recommended, however, since each would require considerable nonrecurring engineering (NRE) expenses, which would make its cost as great as the higher capacity options. Five hardware options were not investigated in detail because of inherent characteristics which made them unacceptable for AN/SLQ-32(V) use. These five are as follows:

1. Magnetic Floppy Disk. Magnetic floppy disks have limited storage density and a relatively slow data transfer rate, and they are easily damaged.

2. Electrically Erasable Programmable Read Only Memory (EEPROM). EEPROM chips have limited speed and storage density. Writing a lengthy set of programs could require hours since the write time is listed in milliseconds per byte. One EEPROM chip can hold approximately four kilobytes of data; consequently, storage of the AN/SLQ-32(V) software would require 750 EEPROM chips. The cost of the chips alone would be $15,000 for each unit, not including packaging, control circuitry, and engineering. The chips would also require periodic replacement since they can accept only a finite number of write cycles before they are unusable.

3. Nonvolatile RAM. Like the EEPROM chips, nonvolatile RAM chips have inadequate speed and storage density for AN/SLQ-32(V) requirements. Another limitation is that each chip's built-in battery is nonrechargeable, thus limiting its lifetime to the lifetime of the battery. (However, battery lifetime might be up to ten years long.)

4. Magnetic Core Memory. Magnetic core memory, already used in the AN/UYK-19, is inadequate as a mass storage device because of its storage density. Two new input/output units containing 47 core memory cards would be required for 1.5 megawords of storage capacity, and they would offer no possibility of further software capability expansion.

TABLE 2. HIGH MEMORY CAPACITY HARDWARE OPTIONS

SYSTEM OPTIONS	AVERAGE DATA TRANSFER RATE (KBYTES/SEC)	MEMORY CAPACITY (MEGABYTES)	MEETS MIL-SPECS	MTBF (HR) MTTR (MIN)	EST. WORST-CASE DEVICE BOUND LOAD TIME (SEC)	COST
HARD DISK						
VRC 8010	625	10	?	10000 hrs 15 min	2	$20,000
VRC 8520	625	10-22	No	10000 hrs 30 min	2	$ 6,000
MILTOPE RD-5/15	625	5-15	Yes	8000 hrs 15 min	2	$24,000
ROLM 4150	390	35.6	Yes	3900 hrs 20 min	2	$36,500
GENISCO EDR-100	687.5	11.22-30.06	MIL-STD-810	~9000 hrs ~15 min (Estimated)	2	$12,000
BUBBLE						
MILTOPE BMS-1000 (MOD)	128	3	Yes	10000 hrs 15 min	6	$40,000
LIBRASCOPE RD-509/G	128	8	Yes	7000-10000 hrs 15 min typ.	6	$190,000
SPERRY/AEDAS	250	4-32	Yes	7390 est. 15 min	3	$100,000 (for 25 to AEDAS (PMA-253))

TABLE 2. (Cont.)

SYSTEM OPTIONS	AVERAGE DATA TRANSFER RATE (KBYTES/SEC)	MEMORY CAPACITY (MEGABYTES)	MEETS MIL-SPECS	MTBF (HR) MTTR (MIN)	EST. WORST-CASE DEVICE BOUND LOAD TIME (SECS)	COST
BUBBLE (Cont.)						
LIBRASCOPE MSS	136	4	Yes	7000-10000 hrs 15 min typ.	5	$90,000
FLOPPY DISK						
MILTOPE DD-400	62.5	6.4	Yes	7000 hrs 15 min	11	$16,900 Extreme Environment $11,400 MIL-SPEC
DYNAMIC RAM WITH BATTERY	813	3+	Based on NRE	10000 hrs 15 min	1	$125/64 kbyte chip+ $21.85/ battery + NRE
OPTICAL DISK (see text)						
BERNOULLI DISK DRIVE						
MILTOPE BDS-501R	625	5	?	10000 hrs 30 min	2	$12,000

TABLE 3. LOW MEMORY CAPACITY HARDWARE OPTIONS

SYSTEM OPTIONS	AVERAGE DATA TRANSFER RATE (KBYTES/SEC)	MEMORY CAPACITY	COST	NRE	DISADVANTAGES
DYNAMIC RAM WITH BATTERY	813	64 KBYTES/CHIP 12 CHIPS=768 KBYTES	$125/CHIP 12 CHIPS=$1500 BATTERY=$21.50 OR LESS	YES	NEEDS BATTERY CIRCUIT
NVRAM	813	8 KBYTES/CHIP 90 CHIPS=720 KBYTES	$ 55.25/CHIP 90 CHIPS=$4972.50	YES	LIMITED CHIP LIFE LOW MEMORY DENSITY SOME HAVE SLOW WRITE TIME
EEPROM	625	8 KBYTES/CHIP 90 CHIPS=720 KBYTES	~$ 57/CHIP 90 CHIPS=$5130	YES	LIMITED WRITE CYCLES 10,000 TYP. LOW MEMORY DENSITY SLOW WRITE TIME
EPROM	488	64 KBYTES/CHIP 12 CHIPS=768 KBYTES	$250/CHIP 12 CHIPS=$3000	YES	HIGH COST FOR LARGER MEMORY NEED UV LIGHT SOURCE ON SHIP TEDIOUS ERASE PROCEDURE
STANDARD BMS-1000 MILTOPE BUBBLE	128	512 KBYTES	~$ 24,000 INCLUDING CONTROLLER	INTER-FACE	COST OF LOW MEMORY CAPACITY IS EQUIVALENT TO HIGH MEMORY CAPACITY OPTIONS

5. Erasable Programmable Read Only Memory (EPROM). EPROM chips require ultraviolet lamps to erase their contents and are relatively expensive (as much as $250 each).

The five other hardware options considered in this investigation were found to be feasible. These options (magnetic hard disk, optical disk, magnetic bubble memory, RAM with battery backup, and Bernoulli disk drive) are discussed in detail below.

MAGNETIC HARD DISK

The magnetic hard disk is an electro-mechanical device which offers dense memory storage and rapid data access and transfer. Its dense storage and rapid access time require that the read heads, which perform the data extraction, be situated very close to the recording medium. If the disk is vibrated, impacted, or accelerated too quickly, the high-speed rotating medium can be damaged by contact with the read heads or the enclosure. Shock and vibration from the firing of 5-inch guns on a Naval ship could destroy a disk not designed to withstand such treatment. Only a very sturdy disk system built to conform to rigid military specifications could withstand the shock and vibration from a ship with 16-inch guns, such as the battleship New Jersey. (Appendix C presents shock and vibration test results from the New Jersey.)

A wide variety of magnetic hard disks is available, but only two are military standard: the UYH-2 and the UYH-3. These disks are large (refrigerator-sized), heavy (~300 pounds), and expensive (~$200,000), making them unrealistic choices except perhaps for the battleships New Jersey and Iowa. This section of the report describes the investigation of some smaller and less expensive commercial hard disks. Table 4 shows a comparison of cost, size, memory capacity, and environmental sturdiness for four of these disks: the Miltope RD-5/15, the ROLM 4150, the VRC 8520, and the Genisco EDR-100. Advertising sheets for the Miltope, VRC, and Genisco disks are included in Appendix A. The ROLM sheet is not included because ROLM copyrights its advertisements.

Any nonmilitary standard hard disk selected for AN/SLQ-32(V) use should first be thoroughly tested on ship or in a simulated environment to ensure that the device can withstand the shock and vibration of the firing of guns.

Miltope RD-5/15

The Miltope RD-5/15 hard disk offers up to 15 megabytes of memory storage, a data access rate of 40 milliseconds (msec), and a data transfer rate of 625 kilobytes per second. These exceed requirements for AN/SLQ-32(V) use.

The Miltope RD-5/15 disk is "militarized," which means that it has been built to conform to military specifications for shock, temperature, and vibration. Militarized does not mean that the disk has passed government tests ensuring this conformity, however. Table 5 lists the requirements for the AN/SLQ-32(V) system. Although the RD-5/15 appears to meet or exceed these requirements, testing is essential if this disk is selected for shipboard use.

TABLE 4. MAGNETIC HARD DISK SPECIFICATION COMPARISON

	MILTOPE RD-5/15	ROLM 4150	VRC 8520	GENISCO EDR-100
COST	$24,000	$36,500	$6,000	$12,000
SIZE	ATR PANEL W 7.5" 8.0" D 13.63" 13.63" H 7.62" 8.62"	W 19.0" D 24.0" H 12.25"	W 8.55" D 16.61" H 7.0"	W 19.0" D 20.0" H 7.0"
WEIGHT	25 lbs	125 lbs	34 lbs	50 lbs
MEMORY CAPACITY	5 to 15 megabytes	35.6 megabytes	10 to 22 megabytes	11 to 30 megabytes
OPERATING ENVIRONMENT				
TEMPERATURE	-30° to 55°C	-30° to 55°C	0° to 55°C	0° to 50°C
RELATIVE HUMIDITY	5% to 100%	MIL-STD-810C CAT 1	5% to 90%	0% to 95%
ALTITUDE	--	--	-1000 to 8000 ft	0 to 1000 ft
SHOCK	15 g for 11 msec	15 g for 11 msec	2 g for 11 msec 2 per second max	20 g for 11 msec
VIBRATION	.075" displacement 5 to 2000 Hz	.075" displacement 5 to 2000 Hz	.01" displacement 5 to 20 Hz	0.1" displacement 5 to 10 Hz
MTBF	8000 hrs	3900 hrs	10000 hrs	~9000 hrs
MTTR	15 min	20 min	30 min	~15 min

TABLE 4. (Cont.)

	MILTOPE RD-5/15	ROLM 4150	VRC 8520	GENISCO EDR-100
SERVICE LIFE	Not Listed	Not Listed	5 yrs or 30000 hrs	Not Listed
NONOPERATING SHOCK	30 g for 11 msec	30 g for 11 msec	6 g for 16 msec	MIL-STD-810 Method 516.1, Procedure V for nonoperating shock
MILITARY STANDARDS CITED	MIL-STD-810 MIL-E-16400 MIL-E-5400 MIL-E-4158 MIL-STD-461 TEMPEST NACSEM 5100	MIL-STD-810C MIL-E-16400 MIL-E-5400	None	MIL-STD-810

TABLE 5. AN/SLQ-32(V) ENVIRONMENTAL REQUIREMENTS (From ELEX-C-241E)

CONDITION	MIL SPEC CITING REQUIREMENTS	EXCEPTIONS TO MIL SPEC REQUIREMENTS

TEMPERATURE — MIL-E-16400

Equipment	Class	Operating	Nonoperating
Interior	4	0°C to +50°C	-54°C to +75°C
Exterior	2	-28°C to +50°C	-54°C to +75°C
Exterior (mast mounted)	2	-28°C to +65°C	-54°C to +75°C

SHOCK — MIL-S-901, Grade A, Class III: None

VIBRATION — MIL-STD-167-1, Type 1

Equipment	Direction Relative to Ship's Heading	Frequency (Hz)	Level (Double Amplitude) mm	Level (Double Amplitude) inches
Band 1 antenna	3 axes	4-10	5.08	0.20
		11-15	1.52	0.06
		16-25	1.02	0.04
Interior	3 axes	4-15	1.52	0.06
		16-25	1.02	0.04
Exterior (except Band 1 antenna)	Vertical, athwart	4-11	2.29	0.09
		12-15	1.52	0.06
		16-20	0.77	0.03
		21-25	0.51	0.02
Exterior (except Band 1 antenna)	Longitudinal	4-15	1.02	0.04
		16-25	0.31	0.012

The Miltope RD-5/15 has the advantage of being cheaper (~ $24,000) and less bulky than the other militarized disk investigated for this report. It has the disadvantage of not having a proven reliability record in government service. ROLM Corporation has agreed with Miltope to develop an interface to the ROLM computer (AN/UYK-19) which would be compatible with the Miltope SCSI interface. At the time of this report, however, the RD-5/15 had not been delivered to ROLM for the engineering work to begin.

ROLM 4150

The ROLM 4150 hard disk offers up to 35.6 megabytes of memory storage, a data access rate of 42 msec, and a data transfer rate of up to 390 kilobytes per second. These exceed the requirements for AN/SLQ-32(V) use.

The militarized ROLM 4150 has been designed and built to conform to rigid military specifications. ROLM products (e.g., AN/UYK-19 computer) have proved their reliability in government service. Since ROLM engineered and produced the AN/UYK-19 computer, the engineering required to interface the computer to the hard disk is minimal. If selected for shipboard use, however, the ROLM 4150 would be difficult to mount because of its relative bulkiness: 125 pounds and 3 cubic feet. It is also more costly ($36,500) than the other disks investigated for this report.

VRC 8520/VRC 8010

The third hard disk investigated, the Vermont Research Corporation (VRC) model 8520, offers up to 22 megabytes of memory storage, a data access rate of 58 msec, and a data transfer rate of 625 kilobytes per second. These exceed the requirements for AN/SLQ-32(V) use.

The VRC 8520 is the least expensive of the hard disks investigated for this report. The basic cost for each unit would be $6000 for the disk, $125 for each cartridge, and $250 for the mounting rack.

Unfortunately, the VRC disk is a "ruggedized" unit. Ruggedized means that the disk is usable in an industrial environment without being shackled to an office worker's desk. It is much less resistant to vibration and shock than the militarized Miltope RD-5/15 and ROLM 4150. Dr. Jon Yagla, an NSWC expert in the area of shipboard shock and vibration, has determined that the ruggedized VRC 8520 could not survive operationally in combat situations, even if it were mounted to dampen vibration and shock.

VRC produces another hard disk, the VRC 8010, with specifications almost identical to the VRC 8520. This disk is presently being modified by ROLM to increase its environmental durability and to facilitate its interface with ROLM military computers. The modification will increase the height and width of its chassis by approximately two inches. Graham Hall, AN/SLQ-32(V) project manager for Raytheon Corporation, has estimated the cost of the modified VRC 8010 to be $20,000 per unit.

Genisco EDR-100

The Genisco EDR-100 hard disk offers up to 30 megabytes of memory storage, a data access rate of 68 msec, and a data transfer rate of 687.5

kilobytes per second. These exceed the requirements for AN/SLQ-32(V) use.

Although the Genisco EDR-100 is classified as ruggedized, it has been designed and built to meet the shock and vibration specifications of MIL-STD-810. These are itemized in its advertisement sheet in Appendix A.

The EDR-100 offers several advantages over the other hard disks investigated. It can be mounted in any orientation, its dual disk drive permits separate storage of classified information, and its price is $12,000.

OPTICAL DISK

Optical disk systems store data by burning the recording medium (i.e., disk) with a high-powered laser, causing pits or blisters on the surface. A lower-powered laser is used to read the recorded data. Data storage and access requires a precise alignment of the laser, mirror, and disk components of the device. This alignment on a nonmilitarized device could be disturbed by the shock and vibration of guns firing. Only a militarized unit should be considered for fleet use.

Two types of optical disk systems are currently in production. Read-only devices are relatively inexpensive, selling for several hundred dollars each. These are not recommended for AN/SLQ-32(V) use, however, since the entire process of software delivery to the fleet would have to be changed. Devices capable of both reading and writing data have been investigated for this report because they would more likely meet fleet requirements.

At present optical disks can be written only once since they are nonerasable. However, the storage capacity of most present optical disks is 1 gigabyte, and this is sufficient for all current AN/SLQ-32(V) programs to be written 300 times on a single disk. This capacity would certainly meet storage requirements for all anticipated software expansion.

The following optical disk systems, listed by manufacturer, were investigated for possible AN/SLQ-32(V) use:

1. RCA. RCA has developed an impressive optical disk system containing 1250 gigabytes of data on 128 optically recorded disks. This system, which was developed for the U.S. Air Force, has a random access time of six seconds or less for any byte. It works in a manner similar to a juke box except that multiple disks can be accessed simultaneously. The unit requires 32 square feet of floor space and costs approximately $1 million dollars.

   RCA is currently developing a smaller-sized militarized single-disk optical system which will be available for $100,000 per unit in 1987. No specifications are readily available for this system.

2. Alcatel Thompson. The GD 1001 produced by Alcatel Thompson has a data access rate between 5 and 200 msec, depending on whether the search is within or outside a current band of tracks. Its data transfer rate is 479 kilobytes per second. The GD 1001 weighs 50 pounds and is approximately the size of a phonograph. It uses both

single-sided and dual-sided disks, and its cost is $13,000 per unit plus $315 for each single-sided disk.

The Combat Systems Engineering branch (N24) of NSWC recently acquired by competitive contracting a GD 1001 as a possible replacement for their RD 358 tape drive system. Personnel from N24 could supply additional information on this optical disk system.

3. Shugart Corporation. The Optimem 1000 manufactured by Shugart has a storage capacity of 1 gigabyte per disk and a data transfer rate of 625 kilobytes per second. Its cost is approximately $13,600 plus $400 for each disk.

4. Storage Technology. An optical disk system produced by Storage Technology has a storage capacity of 4 gigabytes per disk and a data transfer rate of 1500 kilobytes per second. Unfortunately, it costs $130,000 per unit.

5. Sony Corporation. A Sony optical disk system will be available in both 8" and 12" disk sizes in August, 1985. The data access rates are listed as 1.2 seconds across tracks and 0.5 seconds within a track. The data transfer rate is listed as 300 kilobytes per second. The 8" disk system is a compact 14.75" x 6.75" x 7.875". The projected cost is $9,300.

6. Cherokee Data Systems. A 250 megabyte optical disk system being developed by Cherokee Data Systems, a newly-formed optical disk company, will be available in 1987. This unit will be ruggedized and will occupy the space of a standard desk-top floppy disk unit. The projected price for this system is $2,700 per unit.

7. National Memory Systems. National Memory Systems makes a 12" optical disk which uses the Optimem 1000 drive. Its storage capacity is 1 gigabyte, and its cost is $23,500 in quantities of one.

The optical disk systems investigated for this report present two major problems in their consideration for AN/SLQ-32(V) use. First, none of the reasonably priced units currently available are built to military specifications. Second, availability is limited and delivery time is substantial, based on the experience of the NSWC acquisition of the GD 1001. Thus, the optical disk systems do not seem likely candidates for immediate AN/SLQ-32(V) use.

MAGNETIC BUBBLE MEMORY

A magnetic bubble memory system is a high density, solid state, nonvolatile serial read/write storage device. It is compact and reliable, requires no routine maintenance, and can operate under harsh conditions such as high humidity, dust, vibration and shock, and temperature extremes. The basis of bubble memory technology is the existence of magnetic domains within a thin film. The domains shrink to cylindrical "bubbles" in the film when they are exposed to an external magnetic field. A rotating magnetic field is then used to move the bubbles along their data loop.

Bubble memory systems have both advantages and disadvantages over magnetic hard disk systems. Because the bubble memory system is a solid state device, it offers an inherent reliability and sturdiness not offered in the electro-mechanical hard disk. The software required for interfacing bubble memory to the AN/SLQ-32(V) is less extensive than that required for disk because of the sector checking required for disk. On the other hand, bubble memory storage capacity and data transfer rates, although adequate, are not as good as those of the hard disks and optical disks. The cost per unit of storage capacity is substantially more for bubble memory than for disk. Its technology is expanding rapidly, however, and this should drive the costs down.

Only two vendors presently make bubble memory for general use--Motorola and Intel. Sperry uses the Motorola product, which is reputed to offer better functional performance. Librascope uses the more widely sold Intel product.

Three bubble memory systems were investigated for this report and are described below. Three other systems were proposed by manufacturers who could provide the systems.

Librascope Expanded Memory

The Librascope Expanded Memory (RD-509/G) has a storage capacity of 8 megabytes, a data access rate of 40 milliseconds, and a data transfer rate of 1 megabit per second. These meet the requirements for AN/SLQ-32(V) use.

The RD-509/G is 1.48 cubic feet in size and weighs 75 pounds. Because the unit has been built and tested to military specifications (U.S. Army contract DAAK80-79-0016), it should be capable of withstanding the rigors of sea duty. At $190,000 per unit, though, it is too expensive for widespread fleet use. An advertisement sheet for the Librascope Expanded Memory is included in Appendix A.

Librascope Mass Storage Subsystem

The Librascope Mass Storage Subsystem (MSS) is an 8-megabyte bubble memory system being developed for use in the MX Peacekeeper missile, the U.S. Army's Communication Control Switch in the Tactical Fire Support Systems, and the Royal Australian Navy's Mark I Torpedo Fire Control System. Information on this military-standard bubble memory system is included in Appendix A. Librascope has proposed building a similar system for AN/SLQ-32(V) use at a cost of $90,000 per 4-megabyte unit. The price would be prohibitive for widespread fleet use but is worth consideration for battleship use.

Sperry/AEDAS

Sperry is developing a militarized bubble memory system in an Air Transport Receiver (ATR)-sized package for the AEDAS program (PMA-253). The functional features of this device are much better than those of other devices investigated for this report. It will have an NTDS interface, a storage capacity variable from 4 to 32 megabytes, a data transfer rate of 250 kilobytes per second, a data access rate of 12.5 msec, and rapid memory purge at the press of a button. The cost for the four initial units is $700,000.

Twenty-five additional units will be delivered for $100,000 each. If units were purchased in quantity for AN/SLQ-32(V)-equipped ships, the price would probably be further reduced.

Other Proposed Systems

The Miltope BMS-1000 is a militarized bubble memory unit which offers a maximum storage capacity of 256 kilobytes. An advertisement sheet for the BMS-1000 is included in Appendix A. Although the BMS-1000 would be inadequate for AN/SLQ-32(V) use, the Miltope marketing director has indicated that Miltope could produce a similar 3-megabyte unit for approximately $40,000 per unit.

A ROLM sales representative proposed two bubble memory options which ROLM could produce for the AN/SLQ-32(V). It could produce a 4-megabyte system in a half-sized ATR chassis for approximately $50,000 per unit. No operating specifications for this proposed device were offered. The ROLM representative also proposed the installation of two bubble memory cards in two presently empty core memory planes in the AN/UYK-19 I/O boxes of the AN/SLQ-32(V). These two cards would provide enough memory to store the tactical programs and libraries but not the SDT programs. The cost for this proposed bubble memory system would be approximately $700,000 in initial engineering costs and $30,000 for each unit.

RAM INTEGRATED CIRCUITS WITH BATTERY BACKUP

Recent advancements in electronic technology have produced RAM integrated circuit chips with large memory capacities, rapid data access, low power requirements, and low cost. These characteristics make a mass memory storage system using RAM chips a feasible alternative to a hard disk, optical disk, or bubble memory system.

A 3-megabyte mass memory system using low-power (CMOS-technology) dynamic RAM chips would require a constant power supply of only 23 milliamps for data storage. Unfortunately, the refresh circuitry required to sustain the electrical charge necessary for memory retention is not yet readily available on these CMOS chips. If higher-power (NMOS-technology) RAM chips were used, the storage system would require approximately 300 milliamps of continuous current to retain memory.

Because a RAM chip storage system would lose all of its data if power were removed, it would require a rechargeable battery circuit as a backup for the power supply. A nickel cadmium or lead acid battery could provide the power necessary to keep memory intact for hours or days. Gelyte manufactures a 20-amphour rechargeable lead battery which could retain memory for 60 hours. This battery, which sells for $21.85, is 7.5" x 2.3" x 5.7"; but smaller batteries offering fewer amphours are available.

The memory storage capacity of a dynamic RAM system is very attractive. Several manufacturers, including Texas Instruments and Intel, produce 16-pin dynamic RAM chips with a storage capacity of 32 kilobytes per chip. A 3-megabyte system could be developed using 93 RAM chips on five or six printed

circuit cards. If such a system were designed and built to military specifications, the cost for the RAM chips, back-up circuitry, packaging, and engineering might be approximately $30,000 per unit. However, the CMOS technology of these low-power chips is still relatively new, and prices are likely to decrease substantially in the future. Various nonmilitary standard systems are already available off the shelf for under $10,000, but these are not recommended for AN/SLQ-32(V) use in the fleet.

The data access rate of the RAM chip is extremely rapid. For example, the Intel 51C256-L RAM chip has a maximum bit-access rate of 150 nanoseconds. At that rate 813 kilobytes could be accessed in a single second.

The dynamic RAM concept of memory storage offers the reliability of solid state design. Its functional capability, relatively small size, and potential for software expansion make it an attractive option. Future advances in CMOS circuit technology will undoubtedly provide the potential for months of sustained memory from a small battery, even greater storage density and speed, and reduced costs.

BERNOULLI DISK DRIVE

The Bernoulli disk drive system uses the principle of Bernoulli's Law to maintain a close distance and an air bearing between its flexible recording medium and its read/write head. The basic concept of the device is that the flexible recording medium (disk) spins next to a planar surface called the Bernoulli plate. A thin cushion of circulating air between the flexible spinning disk and the Bernoulli plate maintains a relatively constant distance between the two, greatly reducing damage from contamination and from shock and vibration. This concept of data storage and retrieval using Bernoulli's Law was developed by personnel at IOMEGA Corporation.

Miltope Corporation has developed ruggedized versions of this Bernoulli disk drive system. The BDS-5R series of ruggedized disks has impressive characteristics. The BDS-501R stores 5 megabytes of data and has an average access rate of 39 milliseconds and a data transfer rate of 625 kilobytes per second. Larger storage capacities are available in other versions. The BDS-501R weighs twenty pounds and measures 8 1/2" x 9 3/8" x 11 3/4". Its cost is approximately $12,000.

The flexible disk comes enclosed in a hard plastic cartridge which automatically exposes the recording surface when the cartridge is placed in the disk drive. The disk cartridges cost about $50. An advertisement sheet for the BDS-5R series of Bernoulli disk drive systems is included in Appendix A.

CHAPTER 5

INTERFACE CONSIDERATIONS

Regardless of the type of mass storage device chosen, substantial changes would be required to interface the device to the AN/SLQ-32(V) system. The programming and engineering changes described in this chapter would require several man-years of effort and could comprise the greatest cost of implementing mass storage devices in the fleet. The changes will be even greater and more costly if the mass storage devices on the battleships are different from those in the rest of the fleet.

The firmware, software, and hardware of the AN/SLQ-32(V) are presently designed so that all information flows through the RP-16 to the AN/UYK-19 during program load. The program load process is accomplished by two programmable read only memories (PROMs). When the operator presses the Program Load button on the DCC, the RP-16 PROM loads the RP-16 random access memory (RAM) with two programs stored on tape: the primary RP-16 program and the CP-32 debug program. The AN/UYK-19 PROM communicates with the RP-16 PROM and loads AN/UYK-19 memory with the tactical software. The program logic for this loading process (Figure 3) would have to be retained for the purposes of backup and for software delivery via MTC.

At the same time a new loading concept for use with a mass storage device would have to be developed so that the benefits of quick loading and data access could be realized. The new program logic (Figure 4) would have to provide the AN/UYK-19 with a direct connection to the device via the I/O bus or direct memory addressing (DMA) so that the AN/UYK-19 could load itself and all peripheral processors, including the RP-16. The new loading process would involve changes to the present firmware (PROMs), software, and hardware.

SOFTWARE CHANGES

ROLM 1606 Auxiliary Memory Program

A new AN/UYK-19 program must be designed to load the new mass storage device from the old tape system so that the MTC can still be the transportable medium for software delivery. This new program, which is identified in this report as RAMP (ROLM 1606 Auxiliary Memory Program), should also provide several other options to allow full utilization of the new unit:

1. Cataloging new memory unit files. This capability would allow the operator to know the programs available.

```
    RP-16 PROM Program Logic

if No tape is in tape drive then
     if CP-32 program is loaded in RP-16 RAM then
          Execute CP-32 program;

     else

          Dump DCC status to display screen;
     endif

else

     if Operational tape is in tape drive then
          Load RP-16 program from tape;
          Transfer control to RP-16 RAM;
          RP-16 RAM program transfers UYK-19 program data to
               UYK-19 PROM;
          UYK-19 PROM loads UYK-19 program data,
               including loader program (TPLDR), into
               UYK-19 RAM;
          UYK-19 PROM transfers control to TPLDR in UYK-19
               RAM;
          TPLDR loads remainder of operational program
               into UYK-19 RAM and begins program execution;
     endif

     if SDT tape is in tape drive then
          RP-16 PROM loads RP-16 RAM with SDT RP-16 program;
          RP-16 RAM program acts as master program controlling
               running of other SDT programs;
     endif

endif
```

FIGURE 3. PRESENT PROGRAM LOAD PROCESS

```
RP-16 PROM Logic to Incorporate a Mass Storage Device

     if No tape is in tape drive then
          if New memory unit is operational then
               Transfer control to UYK-19 PROM;
               UYK-19 PROM loads new loader program into UYK-19 RAM;
               UYK-19 RAM loader program gets RP-16 RAM program from
                    memory unit and transfers it to the RP-16, loads
                    peripheral processors, if any (Band 1, ADLS, etc.),
                    from the memory unit, loads operational program in
                    UYK-19, loads preselected main and on-line libraries,
                    and begins program execution;

          else

               Give an error message or execute CP-32 program;
          endif

     else -- A tape is in tape drive

          if Tape drive contains operational program or SDT tape then
               RP-16 PROM performs same processing as present
                    program load (see Figure 3);
          endif

          if Tape drive contains RAMP program tape then
               RP-16 PROM transfers control to a RAMP loader
                    section of UYK-19 PROM;
               UYK-19 PROM inputs the RAMP loader, which will load
                    and begin executing RAMP program;
          endif

     endif
```

FIGURE 4. MODIFIED PROGRAM LOAD PROCESS TO INCORPORATE NEW MASS STORAGE DEVICE

2. Transferring programs/files from the storage unit to tape. This capability would permit the creation of back-up tapes from the new unit.

3. Transferring programs/files from tape directly into the new unit.

4. Loading and executing SDT programs from the new unit.

5. Loading and executing tactical programs from the new unit.

6. Designating main and on-line libraries from the selection contained in the new unit. This capability would eliminate all operator loading actions except pressing the Program Load button, an essential feature for combat situations.

The capabilities for auto-dumping and for building and storing libraries on the new unit would also be desirable features.

Tactical Software

The present tactical software would have to be modified in order to provide the option to load and execute RAMP directly from the mass storage device. This capability could be included within ANAL FAB or READ LIBRARY FAB processing. The tape I/O handler would also require expansion to process data from either the tape or the new unit. Finally, the software must provide decision logic for determining the proper source (i.e., tape or mass storage device) for reading in libraries and for loading peripheral processors.

SDT Software

The SDT software would have to be modified in order to execute the diagnostic programs directly from the new unit. NSWC experts have made the following recommendations for maximizing use of the new unit while preserving hardware integrity:

1. Continue to load tests for CTT, DCC, DPU, and associated interfaces from tape.

2. Add a new SDT to check the new unit and its associated interface.

3. Rewrite overlay-segment handling section of full master supervisor, branch and control supervisor, and DPU master supervisor.

HARDWARE/FIRMWARE CHANGES

The actual complexity of the hardware and firmware changes cannot be assessed until a mass storage device has been selected and designed. This section addresses the mounting and interfacing considerations which will be required regardless of the device chosen.

The location of the mass storage device will depend on the device chosen, but it could be critical to the functioning of the system. If it is not located close to the AN/UYK-19, a high-speed fiber-optic communications link might be required. Although (V)3 systems have an empty slot in Rack 2, this space should be reserved for the additional equipment required for at-sea system tests.

Interfacing the new device to the AN/UYK-19 I/O bus will require a modification of both the RP-16 PROM and the AN/UYK-19 PROM. The RP-16 PROM resides in two 1-kilobyte chips (U12 and U13) on the ROLM interface card (Figure 5). Only 14 words remain unused in these chips. Since the card offers no space for additional chips, present chips must be replaced with new chips offering denser memory storage in order to do the new processing. This modification might also involve backplane wiring changes in the DCC. The AN/UYK-19 PROM must be replaced with a new PROM containing the firmware to accommodate the storage device. However, the special interfacing required between the storage device and the AN/UYK-19 could be located in the new unit, eliminating the need for further AN/UYK-19 PROM modification.

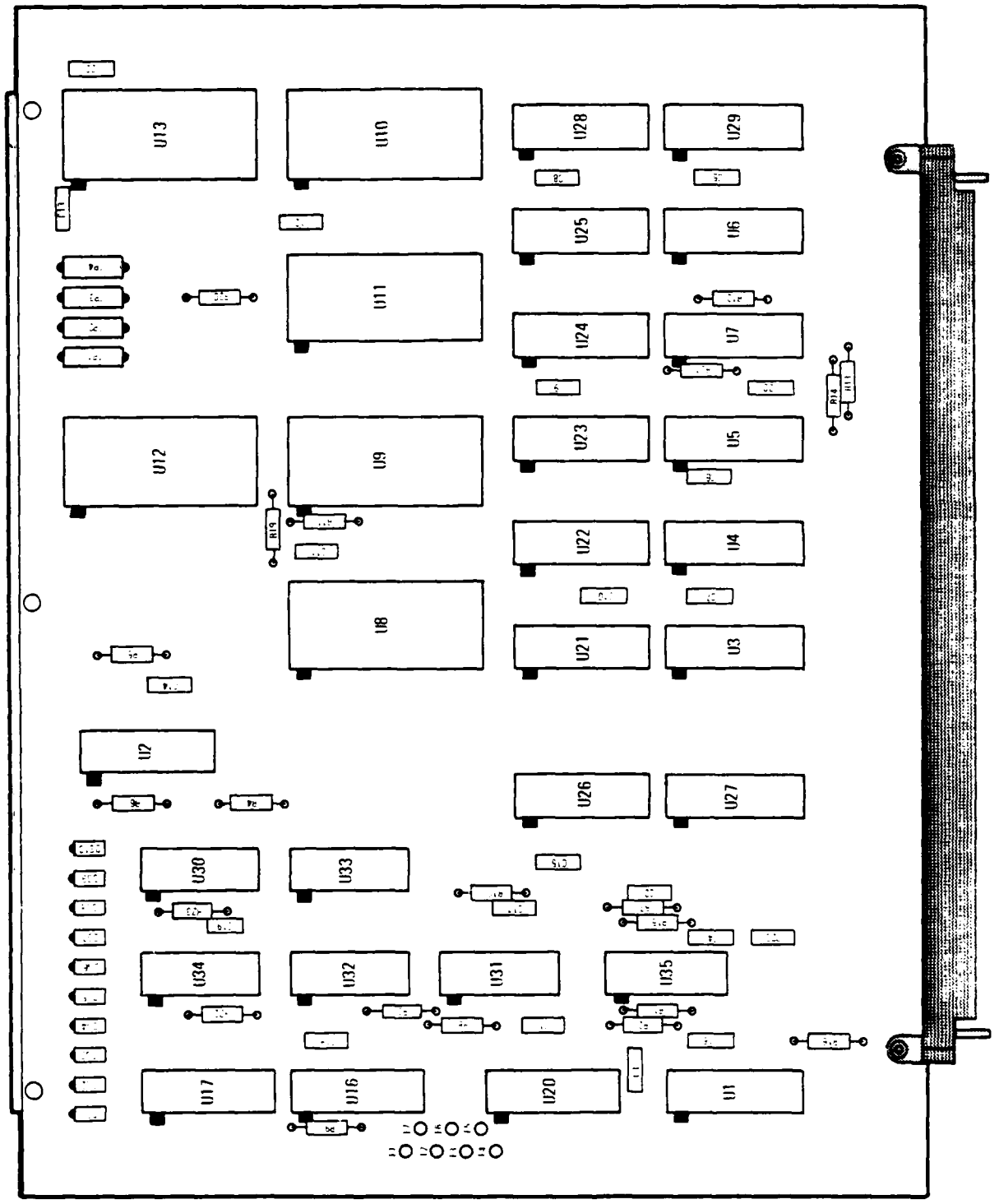


FIGURE 5. ROLM INTERFACE CARD CONTAINED IN RP-16

CHAPTER 6

CONCLUSIONS

The investigation conducted for this report has established a definite need for a mass memory storage device for AN/SLQ-32(V) use. Present program loading requires more than a minute, and future software expansion could extend that time to five minutes or more. This time span could be fatal in a combat situation.

The most important considerations in reducing current load time are storage capacity and data access and transfer rates. Storage capacity should be sufficient to store all current and future tactical and diagnostic software. Data access and transfer should be accomplished in ten seconds or less. Another important consideration for a mass memory storage system is its reliability. Once a device of this type is implemented, its uses may expand to the point where the AN/SLQ-32(V) system could not function without it. Other considerations in this investigation included the size of the device, the cost per unit, and the ease of installation.

Modification of the present magnetic tape system would not reduce load time sufficiently. Storage density and data transfer rates could be increased, but the operator handling and rewinding times inherent to the tape system cannot be improved.

Five hardware options were investigated in detail and were found to be feasible in improving program load time, but none of these were ideal. Magnetic hard disks are readily available but may not be durable enough in a high shock and vibration environment. Optical (laser) disks offer enormous storage capacities; however, they are relatively untried devices, and they require expensive write-once disks. Magnetic bubble memory devices have low maintenance requirements but are very expensive. Dynamic RAM with battery backup offers great potential in speed, sturdiness, and reliability; but no militarized systems with sufficient storage capacities are available. The Bernoulli disk is most promising with its large storage capacity, fast data access and transfer rates, resistance to shock and vibration, and low cost. Testing for military use has not yet been completed, however.

Regardless of the type of device or devices selected for fleet use, considerable changes to the software, firmware, and hardware will be required. These changes will be even greater if one type of device is selected for battleships with extreme shock and vibration conditions and another type is selected for the rest of the fleet. Program load, which now flows from the magnetic tape through the RP-16 PROM to the AN/UYK-19 computer, must be changed to permit a direct connection between the new storage device and the

AN/UYK-19. At the same time, the current loading method must be retained for the purposes of program backup and software delivery. The engineering and programming efforts required to accomplish these changes are likely to comprise the greatest cost of implementing mass storage devices in the fleet.

CHAPTER 7

RECOMMENDATIONS

As a result of the investigation conducted for this report, the following recommendations are made:

1. Any device selected for use in the fleet must be tested to military specifications to withstand extreme shock and vibration conditions.

2. A single type of device should be selected for both battleships and other ships in the fleet in order to prevent possible software and hardware incompatibility problems.

3. The present method of software delivery via magnetic tape cartridges should be retained.

4. The storage capacity of the selected device(s) should be great enough to contain both the tactical and the diagnostic software.

5. The greater storage capacity should not be used to increase the size of the emitter threat library since additional emitters increase, rather than decrease, ambiguities. The size of the threat library should only be increased if more or better discriminants become available.

6. If sufficient time and money are available, some or all of the most promising hardware options should be prototyped. These include the Miltope, Genisco, and VRC magnetic hard disks, the Alcatel Thompson optical disk, the dynamic RAM memory system, and the Miltope Bernoulli disk.

7. As an alternative to prototyping, the U.S. Navy could advertise a "Sources Sought" for a mass memory storage device which meets the required specifications.

8. Competitive contracting should be used for the production contract in order to obtain the optimum cost/performance ratio.

NOMENCLATURE

ADLS	Automated Decoy Launching System
AN/UYK-19	ROLM model 1606 computer
ATR	Air Transport Receiver
CMOS	Complementary metallic oxide semiconductor
CP-32	AN/SLQ-32(V) debug program
CRT	Cathode ray tube (display screen)
CTT	Cartridge Tape Transport unit
DCC	Display and Control Console
DMA	Direct memory addressing
DPU	Digital Processing Unit
ECM	Electronic countermeasures
EEPROM	Electrically erasable programmable read only memory
EPROM	Erasable programmable read only memory
EW	Electronic warfare
MSS	Mass Storage Subsystem
MTC	Magnetic tape cartridge
NMOS	Noncomplementary metallic oxide semiconductor
NRE	Nonrecurring engineering (expenses)
NSWC	Naval Surface Weapons Center
NTDS	Naval Tactical Data System
PROM	Programmable read only memory
RAM	Random access memory
RAMP	ROLM 1606 Auxiliary Memory Program
RP-16	Microprocessor located in DCC
SDT	System Diagnostic Test
UYH-2 and UYH-3	Magnetic hard disks (military standard)
VRC	Vermont Research Company

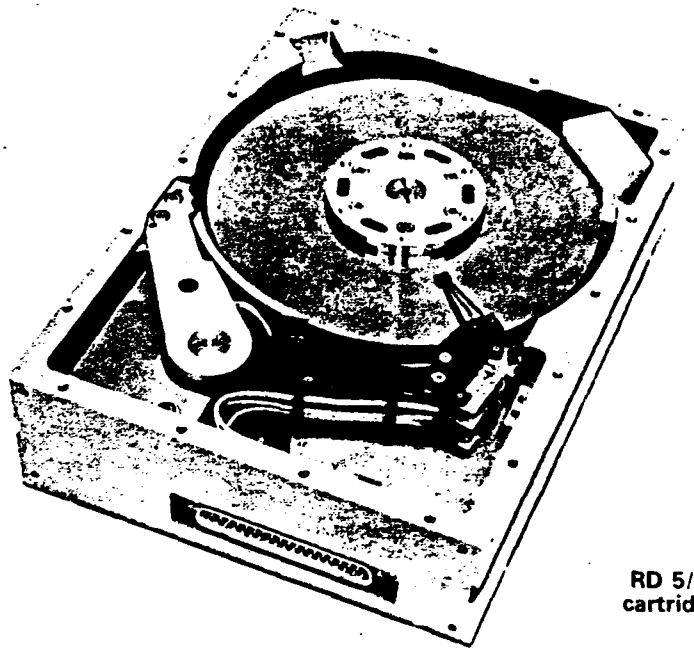
APPENDIX A

SUPPLEMENTARY TECHNICAL INFORMATION

ON MEMORY STORAGE DEVICES

RD-5/15

CARTRIDGE-LOADED WINCHESTER DISC DRIVE



RD 5/15 cartridge

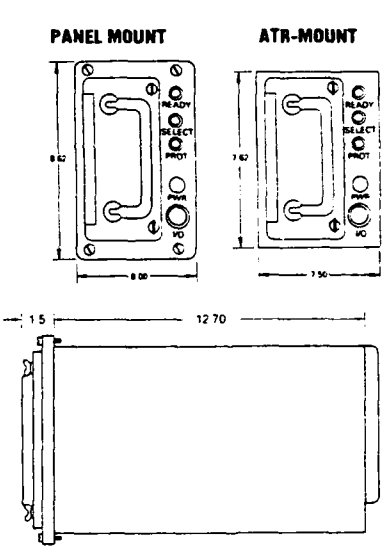
DESCRIPTION

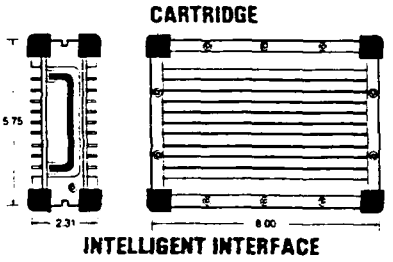
Miltope's RD-5/15 is a cartridge loaded Winchester Technology Disk Drive designed for high speed mass data storage for military computers. The random access memory device stores up to 15 megabytes with an average access time of 40 milliseconds. The system has an intelligent interface that allows easy system integration to the host computer.

Each RD-5/15 cartridge is configured to allow complete plug-in interchangeability, thereby providing the user with a data storage medium that features manual interchange of files.

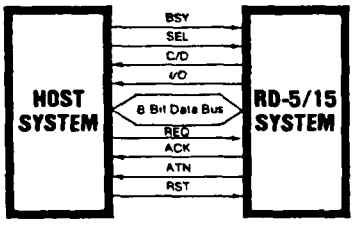
The cartridge load capability eliminates the need for program-loading devices such as magnetic tape or floppy discs, thereby dramatically improving "booting" time. A compact size and full militarization makes the RD-5/15 ideally suited for airborne and ground mobile applications.

OUTLINE DIMENSIONS





INTELLIGENT INTERFACE



FEATURES

- Winchester Disk Technology
- Up to 15 MBYTES Capacity
- Compliance to MIL-E-16400/MIL-E-5400/MIL-E-4158
- Removable, Sealed Cartridge
- Fast Access Time, 40 MS Average
- Intelligent Interface
- Compact Size, ATR or Panel Mount

RELIABILITY

Mean-Time-Between-Failures (MTBF)	8000 hours
Mean-Time-Between-Repair (MTTR)	15 minutes

ERROR RATES

Recoverable (soft)	1 in 10^9 read
Non-recoverable (hard)	1 in 10^{11} read
Seek errors	1 in 10^6 read

INTERFACE

The intelligent interface of the RD-5/15 allows easy interfacing to most host computers. Formatting, error detecting/correcting, addressing, and device controlling is contained within the RD-5/15. Data communication with the host computer bus is accomplished via a host adapter which is normally embedded within the host computer chassis.

PHYSICAL DIMENSIONS

Panel mount	8.0"W × 8.62"H × 13.63"D
ATR mount	7.50"W × 7.62"H × 13.63"D
Power requirements	115 VAC/48-440 Hz single phase optional
Optional	28 VDC
Power dissipation (drive & formatter)	100 watts
Weight (ATR configuration)	25 lbs. max.

CONFIGURATIONS:

RETMA rack	Three RD-5/15 cartridges and electronics can be mounted in 19" RETMA enclosure
Full ATR	Dual RD-5/15 cartridges and electronics can be mounted in a one ATR chassis

FORMATTER

Bus type	Per ANSI X3T9.2 (SCSI)
Format code	MFM encode/decode
Seek and verify	Automatic
Error handling	Auto error detect/correct up to 8-bit burst
Multi-sector transfer	Auto switch to next head on cylinder
Sector size	256 or 512, jumper selectable
Sector buffer	Full sector buffer I/O
Sector interleaving	Programmable
Multi-porting	Up to four computers
Self-test	Internal diagnostics

PERFORMANCE/FUNCTIONAL

Capacity, formatter	5.24 mbytes (RD-5) 15.72 mbytes (RD-15)
Platters	One (5.24 megabytes) Two (15.72 megabytes)
Media	5.25" Plated disc
Access time	10 ms, track-to-track 40 ms, average 8.3 ms, latency
Transfer rate	5 mbps
Rotational speed	3600 rpm
Record density	10,000 frpi, max.
Track density	680 tpi
Cylinders	640
Heads	Two (RD-5) Four (RD-15)

ENVIRONMENTAL

Temperature,	
Operational	−30°C to +55°C
Storage	−62°C to +85°C
Humidity	5% to 100%
Altitude	−1300 to 50,000 ft.
Vibration, Operational	.075 DA to 3 G's, 5-2,000 Hz
Non-operational	5 G's, 5-2,000 Hz
Shock, Operational	15 G's, 11ms
Non-operational	30 G's, 11ms
Bench handling	Per MIL-STD-810
Sand Salt Spray	Per MIL-STD-810
EMI compatibility	Per MIL-STD-461
Tempest, design	NACSEM 5100

6 83

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TEL 516-420-0200 TWX: 510-221-1803

MILTOPE CORPORATION

VERMONT RESEARCH CORPORATION
PRECISION PARK
NORTH SPRINGFIELD
VERMONT 05150
TEL. 802/886-2256
TWX: 710/363-6533

MODEL 8520
8" CARTRIDGE
DISK DRIVE

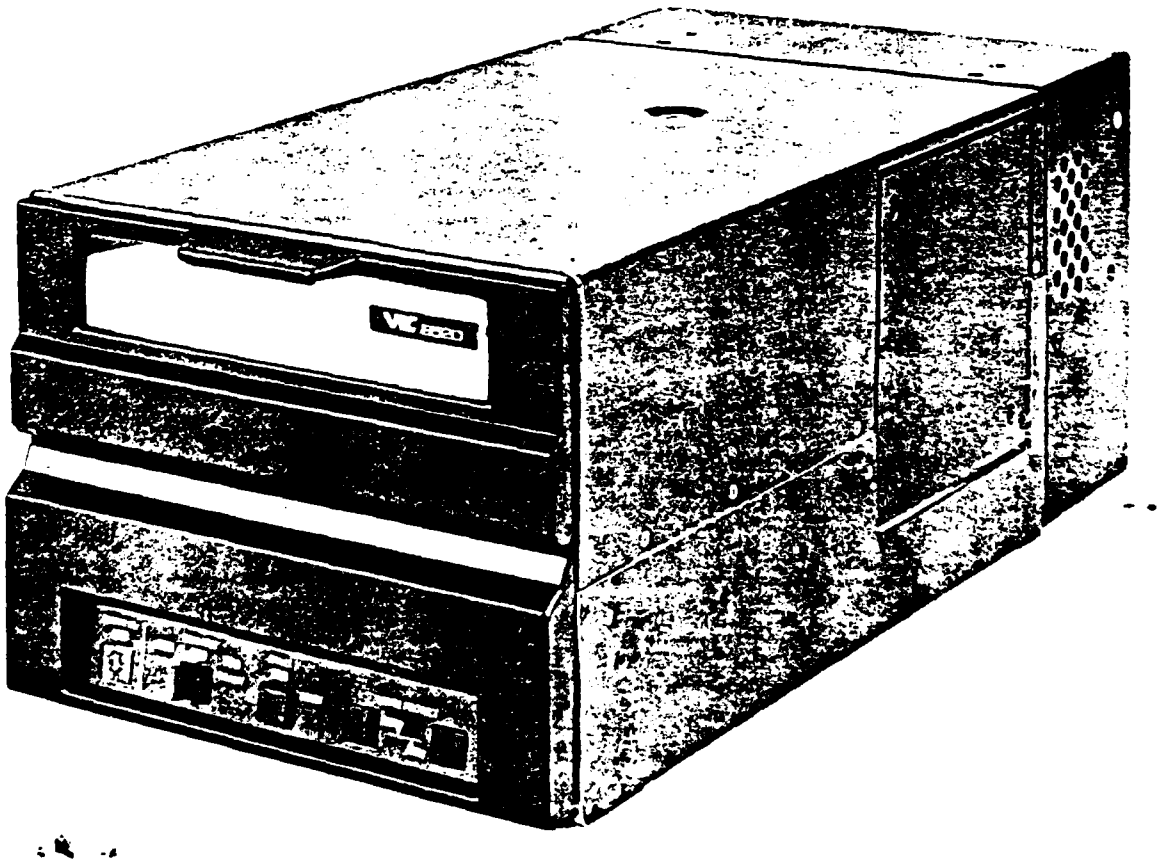
- 22 Megabyte Fixed/Removable 8-inch Hard Disk Drive
- Non-contact heads fly twice as high as heads on other cartridge drives
- Closed-loop air filtration and self-sealing cartridge
- Wide operating temperature range (0° to 55°C)
- Embedded servo head positioning system
- A selection of interfaces, controllers, and mounting options
- Complete memory package with power supply operates from power sources worldwide and meets FCC and VDE radiation specs

The 8520 is a rugged 22 megabyte fixed/removable eight-inch hard disk drive. It is backed up by VRC's 23 years experience designing and buildng memories for customers worldwide.

Non-contact heads which fly twice as high as those on other cartridge drives automatically lock in the retracted position when power is removed or interlocks are violated. This feature works hand-in-hand with a closed-loop air filtration system and a self-sealing removable cartridge to ensure reliability and long life.

The embedded servo closed-loop head positioning system enhances data reliability and guarantees quick reliable cartridge exchange in spite of ambient temperature variations from 0° to 55°C.

The 8520 is a complete memory package which contains all drive electronics, power supply, cooling fan and provision for mounting interfaces or controllers inside. It operates from power sources worldwide and meets FCC and VDE radiation specifications.



MODEL 8520
8" CARTRIDGE DISK DRIVE SPECIFICATIONS*

DATA CAPACITY:	Unformatted	Formatted
Drive	22 Megabytes	19.4 Megabytes
Removable Cartridge	11 Megabytes	10.0 Megabytes
Fixed Disk	11 Megabytes	10.0 Megabytes

DATA ORGANIZATION:	
Disks	2
Data Surfaces	4
Heads/Surface	1
Track/Surface	596
Track/Inch	500
Sectors/Track	32
Data Bytes/Sector	256
Bit Density	6000 BPI Max.

MEDIA:	ANSI X3B7/1981-16, Cartridge with 200 mm OD x 63.5 mm ID oxide coated disk.

PERFORMANCE:	
Access/Seek Time	
One Track Seek	15 msec.
Average Seek	55 msec.
Full Stroke Seek	80 msec.
Ave. Rotational Latency	8.3 msec.
Spindle Speed	3600 RPM
Transfer Rate	5.0 Megabits/Sec. (625K bytes/sec.)

START TIME:	30 secs.

STOP TIME:	20 secs.

ERROR RATES:	
Recoverable	1 in 10^{10} bits tranferred
Unrecoverable	1 in 10^{12} bits transferred
Seek Error	1 in 10^{6} seeks

RELIABILITY:	
MTBF	10,000 hrs.
MTTR	30 minutes
Service Life	5 years or 30,000 power-on hours

POWER REQUIREMENTS:	
DC	+24 VDC +5VDC ±15VDC
AC (with optional power supply)	117VAC ± 10%, 60 Hz ± 6% Start 3.4A, Run 1.5A 230VAC ± 10%, 50 Hz ± 6% Start 1.7A, Run 0.76A

HEAT DISSIPATION:	130 watts (with VRC pwr. sup.)

DIMENSIONS:		
Width	8.55 in.	(21.72 cm)
Depth	16.61 in.	(42.2 cm)
Height	7.0 in.	(17.78 cm)
Weight	34 lbs.	(15.5 kg)

OPERATING ENVIRONMENT:	
Temp. Range	0 to 55°C (32° to 130°F)
Relative Humidity	5% to 90% (no condensation)
Altitude	– 1,000 ft. to 8,000 ft. (– 300 m to 2400m)
Shock	Maximum 2 g 11 millisec; ½ sine-pulses; if continuous, not more than 2 per sec.
Vibration	Displacement - maximum .01 in. (.254 mm), Double amplitude, 5-20 Hz Acceleration-maximum .20 g, 20-300 Hz

NON-OPERATING ENVIRONMENT:	
Temp. Range	– 35° to 70°C (– 31°F to 158°F)
Relative Humidity	5% to 90% (no condensation)
Altitude	– 1,000 ft. to 35,000 ft. (– 300m to 10,800m)
In Transit (pkgd)	maximum 6 g 16 millisec., duration ½ sine-pulses; if continuous, not more than 2 per sec.
Vibration	Displacement-maximum .05 in. (1.27 mm), Double amplitude, 5-9 Hz Acceleration-maximum .20 g, 9-300 Hz

Specifications subject to change.

VRC *Memory products for systems that can't stand failure*

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January 1984

ADVANCE PRODUCT INFORMATION
GENISCO MEMORY PRODUCTS CORPORATION

EDR-100 "TWINCHESTER" Ruggedized Dual Winchester Disk System

Description

The EDR-100 is a ruggedized dual 5¼ inch Winchester disk drive system which provides non-volatile storage of up to 30.06 megabytes of formatted data per system (15.03 megabytes per drive). It is completely self-contained with power supply and interface logic, and is rack-mountable. ST-506 or LSI-11 Multibus interfaces are standard, and other interfaces can be configured upon request.

Each drive is individually sealed and ruggedized. Each is removable from the main system and can be replaced by any other EDR-100 drive. The EDR-100's dual Winchester drives can be configured to operate as individual drives, redundant drives or daisy-chained drives. These configurations are totally software-transparent, with serial recording, simultaneous recording or data dumping under software control.

Rugged components and construction are used throughout the system and the EDR-100 has successfully passed tests within the system's environmental envelope. Electronics are designed as replaceable circuit card assemblies.

Three different media capacities of approximately 6, 12, and 19 megabytes unformatted are available. In the event drives of different capacities are needed after initial application, drives can be freely interchanged without changing chassis, controller or interfaces.

EDR-100 "TWINCHESTER" Ruggedized Dual Winchester Disk System

System Features

- ☐ Ruggedized
- ☐ Interchangeable Media
- ☐ Portable Media
- ☐ Self-contained
- ☐ Three data capacities
- ☐ Non-volatile
- ☐ Modular electronics
- ☐ Standard interfaces

Applications

- ☐ Large and stable ship, aircraft or vehicle-mounted systems
- ☐ Geodetic and seismic data recording
- ☐ Well logging
- ☐ NC machine tool and severe-environment industrial settings
- ☐ Robotics
- ☐ Other military and harsh-environment applications

Specifications

Drive Capacity

Unformatted	*Formatted*
6.375 Mbytes	5.01 Mbytes
12.75 Mbytes	10.02 Mbytes
19.14 Mbytes	15.03 Mbytes

System Capacity

Unformatted	*Formatted*
12.75 Mbytes	10.02 Mbytes
25.50 Mbytes	20.04 Mbytes
38.28 Mbytes	30.06 Mbytes

Performance:

Rotational Speed 3600 RPM

Transfer Rate
687.5 Kbytes/second

Access Times

Track to Track	18.5 ms
Average	68.0 ms
Maximum	120.0 ms
Average Latency	8.3 ms

Power Requirements:

Voltage	115V AC ±10%
Frequency	48 to 450 HZ
Phase	Single (3 Wire)
Amps	1.2 A

Environmental Specifications

Altitude:
MIL-STD-810 Method 500, Procedure I
Operating, to 10,000 feet (3,000 meters)
Non-operating, to 50,000 feet (15,000 meters)

Low Temperature:
MIL-STD-810 Method 502, Procedure I
Operating, 32°F (0.0°C)
Non-operating −40°F (−40°C).

High Temperature:
MIL-STD-810 Method 501, Procedure II
Operating +122°F (+50°C)
Non-operating +160°F (+70°C)

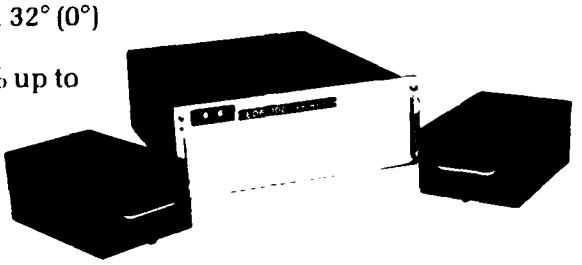
Humidity:
MIL-STD-810 Method 507, Procedure II
Operating to 95% from 32° (0°) to 80°F (27°C)
Non-operating to 100% up to 80°F (27°C) (with no condensation)

Shock:
MIL-STD-810 Method 516.1, Procedure I and V
Operating (Procedure I) 20g 11 msec. half-sine wave (may exhibit degradation in performance during the shock period with no physical damage).
Non-operating (Procedure V) Wooden bench top service.

Vibration:
MIL-STD-810 Method 514, Procedure X and Method 514.1 Procedure IX
Operating (Method 514, Procedure X) 0.10 inch double amplitude 5 to 10 Hz, 0.5g's 10 to 44 Hz, 0.005 DA 44 to 67 Hz, 1.25 g's 67 to 300 Hz. May exhibit degradation of performance during vibration period.
Non-operating (Method 514.1 Procedure IX) 0.10 inch double amplitude 5 to 10 Hz, 0.5g's 10 to 44 Hz, 0.005 DA 44 to 67 Hz, 1.25g's 67 to 300 Hz.

Orientation:
Any position

Specifications subject to change without notice



GENISCO
MEMORY PRODUCTS CORPORATION

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BUBBLE MEMORY RELATED EXPERIENCE

Librascope's Division's extensive experience with bubble memories began in 1978, then aimed toward memory for battle-field communication equipment. During 1980 the 1 megabit Intel module was interfaced and tested and during 1981 system implementation using the Intel bubble were developed, and hardware built and demonstrated. 1983 marked the Qual Testing and delivery to the U. S. Army of the 8 Megabytes TCS Bubble memory system described below.

SINGLE SUBSCRIBER TERMINAL PROGRAM (SST)

Librascope is presently under contract (Contract Number DAAK80-80-C-0284) to the U.S.Army CECOM, Fort Monmouth, New Jersey, for the development of the SST which incorporates a bubble memory cassette. Forty pre-production models are in various stages of tests.

The bubble is an ideal choice for implementation of a cassette-based program because of its non-volatile storage capability. The cassette design is based on the Intel 1-megabit bubble module and chip set. The selected design contains two bubble modules giving a memory capacity of two million bits.

TACTICAL COMPUTER SYSTEM PROGRAM (TCS)

Librascope is also under a production contract to the U.S.Army CECOM, Fort Monmouth, New Jersey for RD-509/G 64-megabit (8 Megabyte) mass memory units with custom I/0 design interfacing with the TCS. The development was under contract number DAAK80-79-0016. The basic building block selected for the mass memory is a single bubble memory controller (BMC) and eight 1-megabit bubble modules (Intel 7110) and their associated support chips, four bubble modules per 6 x 9 inch card.

COMMUNICATION CONTROL SWITCH (CCS)

The CCS Program (Army) was awarded to Librascope in June of 1982 and contains a bubble memory. The CCS will be used in TACTICAL FIRE Support Systems (TFS). This CCS utilizes two of the 6 x 9 bubble cards (1 Megabyte) of the RD-509/G Magnetic Bubble Recorder Reproducer "imbedded" in this CCS system.

ROYAL AUSTRALIAN NAVY LARGE PLASMA PANEL COMMAND DISPLAY

A one megabyte imbedded bubble memory is included in a modification to the RAN's operational Mark I Torpedo FCS, which will provide a 17 inch plasma panel display in the submarine command center.

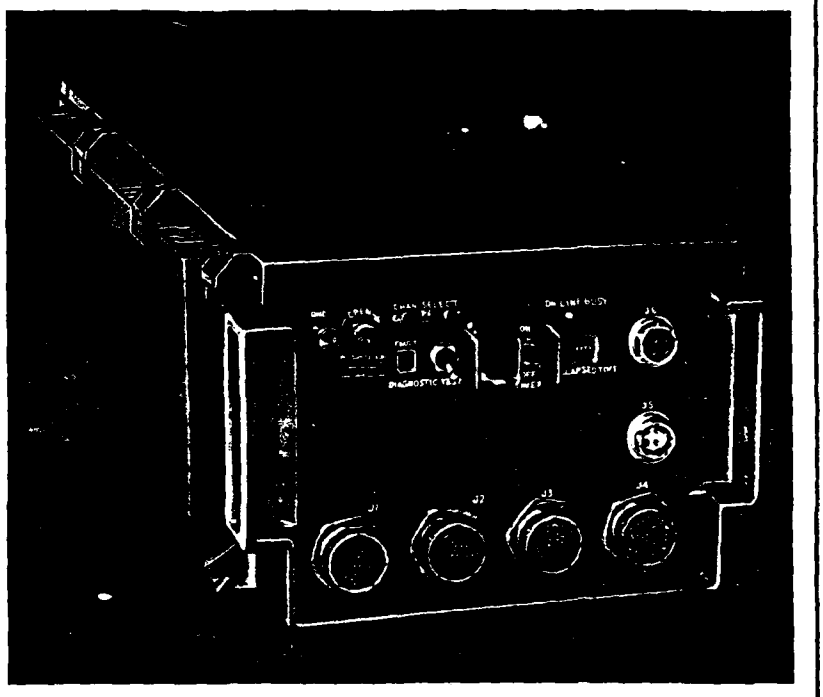
MX PEACEKEEPER COMMAND, CONTROL AND COMMUNICATIONS

Librascope has been awarded a $4.3 million contract by GTE to provide Militarized Mass Bubble Memory Systems for the Peacekeeper Program.

GTE's Strategic Systems Division in Westborough, Mass. is prime contractor to the U.S.Air Force Ballistic Missile Office for the Peacekeeper command, control, and communications system in which the bubble memory systems will be used. The Air Force will use the bubble memories in both ground and air applications.

LIBRASCOPE

Expanded Memory



DESCRIPTION

The Expanded Memory is a *smart* non-volatile modular mass memory containing a dedicated microprocessor and using bubble memory for the non-volatile storage medium. System design is based on 0.5 megabit modules, each contained on a single 6" x 9" PC card. Memory capacity is expandable from 0.5 to 8 megabytes in 0.5 megabyte increments.

The Expanded Memory is comprised of three functional sections, each containing 6" x 9" PC cards: I/O interface, microprocessor with RAM and ROM memory, and non-volatile bubble memory. For operation below −20 ° C. a temperature control function is provided. A regulated power supply is included. Modular design makes the unit easily adaptable to a variety of applications by replacement of the I/O cards for different interface requirements, or by replacement of the microprocessor and/or its firmware for different memory management requirements. The system includes diagnostics and emergency erase features.

Mechanical design of the memory permits the installation of twenty-two 6" x 9" PC cards. In the initial configuration the card allocation is as follows:

	Cards
8 megabyte bubble memory	16
LSDB/HSDB serial I/O	2
6809 processor 7 buffers	1
22K bytes RAM and 24K bytes ROM	1
Heater control	1
Spare	1

The motherboard is laid out for a 16-bit bus allowing a direct plug-in replacement of the 6809 processor card with a 68000 version. The memory card allows room for expanding to 22K (16-bit) words of RAM and 24K words of ROM when the 16-bit bus is used. Addition of a spare card allows an increase of 28K words of RAM.

Modular design of the system architecture allows a variety of I/O requirements to be met by replacement of the I/O cards and maintaining the same DMA transfer for the I/O to and from the RAM buffer. Interface options include the GYK-12 and the 1666B. A dual port system can be implemented by removal of one megabyte of bubble memory (two cards) and replacement with a second set of I/O cards. Both ports have access to the total bubble memory.

DESIGN CHARACTERISTICS (BASIC DESIGN)

Memory capacity: 8 megabytes max.

I/O Data Transfer Rate:

High speed: 1 megabit/sec continuous. 8K byte bursts at 2 megabit/sec

Low speed: 333K bit/sec continuous

Access Time: 40 ms average, 80 ms max.

Emergency Erase: 2 minutes for 8 megabytes

Page Size: 1K bytes based on 1 megabit data rate (16 bubbles running in parallel).

Operating Temperature Range (without the use of heaters): −20 ° C. to +63 ° C. ambient. With the use of built-in heaters, operation is extended to −45 ° C.

Storage Temperature Range: −55 ° C. to +100 ° C. (Without loss of stored information).

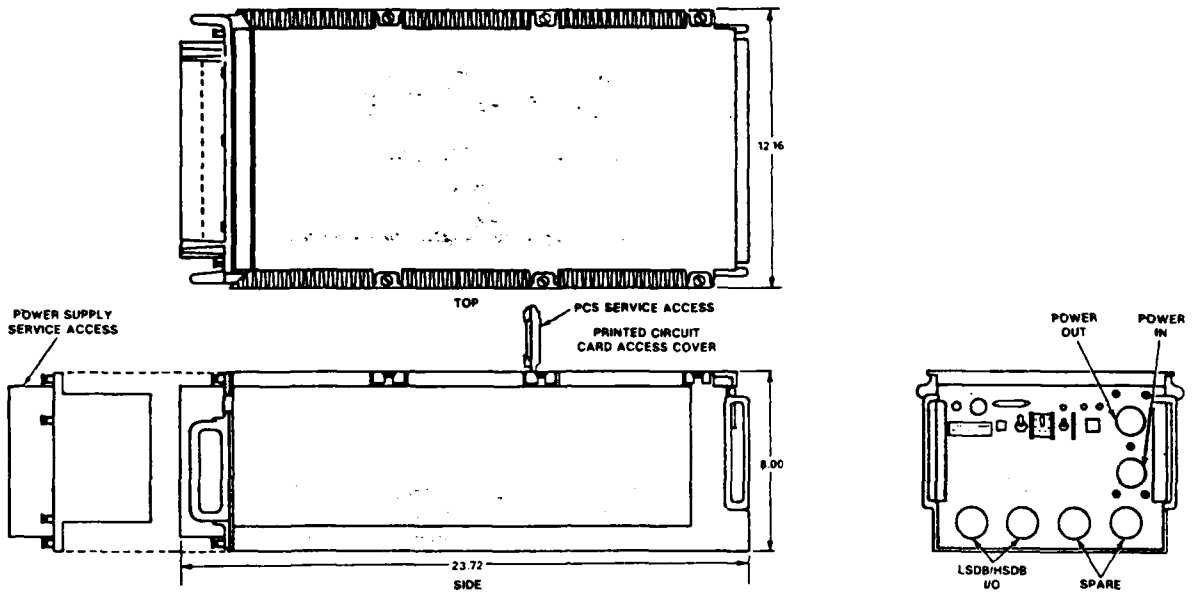
Input Power (including maximum heater power): 25 amps at 22 to 36 VDC unregulated.

Power Allocation: 180 watts operating (16 bubbles reading or writing in parallel). 30 watts standby (Bubbles not operation). Heater power used is controlled by microprocessor and depends on temperature and whether system is in standby or operating. Maximum heater power is 500 watts. Warm up time from −45 ° C. approximately 10 minutes.

Unit Size: 8 in. H x 12.5 in. W x 25.5 in. D.

Unit Weight: 75 lbs.

MOUNTING FACILITIES



ENVIRONMENTAL SPECIFICATIONS

Altitude: Operation to 10,000 ft.
Transport to 50,000 ft.

Temperature: MIL-STD-810B, Method 501, Procedure II.

Operational −45°C to +60°C.
Storage −57°C to +71°C.

Humidity: MIL-STD-810B, Method 507, Procedure III.

Vibration: 5.0 to 5.5 Hz at 1.0 inch double amplitude.

5.5 to 30 Hz at 1.5G.

30 to 48 Hz at 0.036 inch double amplitude.

48 to 500 Hz at 4.0G.

Shock: MIL-STD-810B, 15G, 11 millisecond shocks on three mutually perpendicular axes.

Immersion: MIL-STD-810B, Method 512, Procedure I.

Rain: MIL-STD-810B, Method 506, Procedure I.

Sand and Dust: MIL-STD-810B, Method 510, Procedure I.

Salt Fog: MIL-STD-810B, Method 509, Procedure I.

Acoustic Noise: SCL-1280D, Para 4.7.4

Fungus: MIL-STD-810B, Method 508.

Bench Handling: MIL-STD-810

Electromagnetic Interference: MIL-STD-461, Notice 4

CE01 CS01 RE02 RS03

CE04 CS02 RE02.1 RS03.1

CS06

Chemical, Biological, Radiological: TM3-220

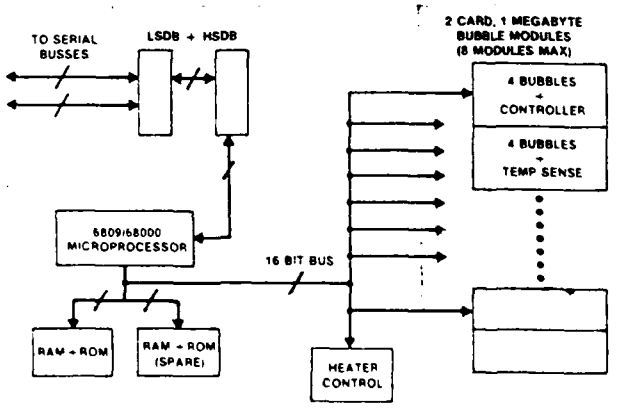
Other: Meets TEMPEST and Nuclear Survivability Requirements.

POWER REQUIREMENTS

Voltage: 22 to 30 VDC vehicular power per MIL-STD-1275 (AT) except for Para. 5.4 Abnormal System Without Battery Support.

22 to 30 VDC mobile generator power per MIL-STD-1332B, Class 2C.

FUNCTIONAL DIAGRAM



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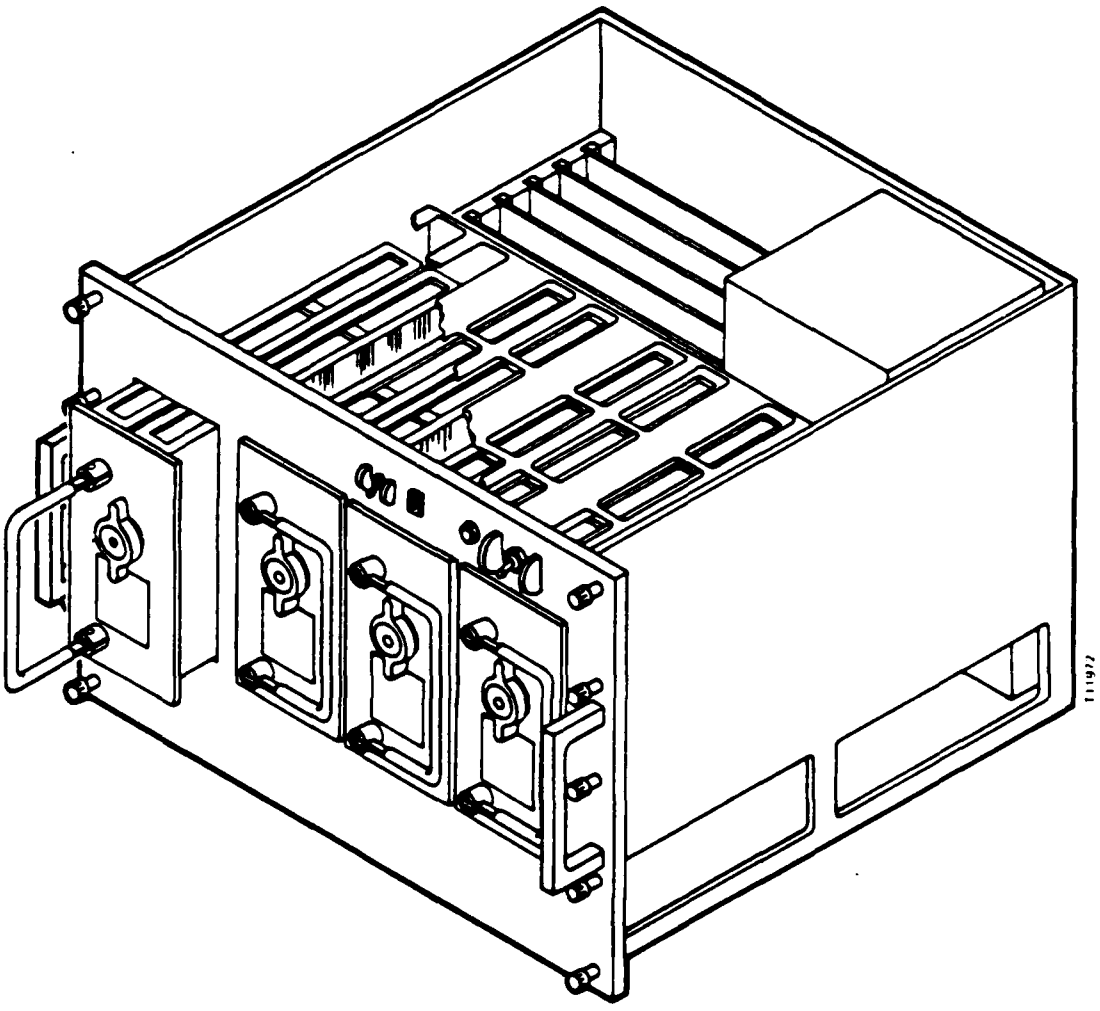
ATT22 AL 1196 ISSUED 5 82 5M

The Mass Storage Subsystem (MSS) features the use of off-the-shelf bubble memory subassemblies. The proposed MSS, as shown in Figure 2.1, consists of four easily removeable 2-Megabyte memory cartridges (front accessed), a power On/Off switch and indicator, and a BIT switch and indicator, all clearly visible and accessed on the front panel. The microprocessor, RAM/ROM, and I/O cards, as well as the power supply are located to the rear of the memory cartridges, and are accessible from the top of the open chassis. The chassis is designed to allow free air flow upwards thru the equipment with the 200 CFM air available at an assumed 64°C maximum. EMI/RFI considerations are taken into account at the front panel and assumes enclosure within the customer provided 19-inch rack.



Proposed Design Approach for Mass Storage Subsystem

All of the above assemblies are off-the-shelf equipment, except the chassis and one "Buffer Card" and modifications to the power supply to accommodate 60 Hz input power and a larger output power capability of +5V DC and +12V DC.

The new Buffer Card serves to facilitate insertion and removal of the memory cartridges into the active data bus and control lines. Also on the Buffer card is logic for BMC select, multiplexing of DMA and I/O, and the determination of memory cartridge status (such as: "Cartridge Inserted" and "Write Lock-out").

The two I/O cards are NTDS type C (ANEW), to MIL-STD-1397. Each I/O is on a first come, first serve basis. Each has an input and an output MS connector at the rear of the chassis. A fifth MS connector is for the 115V, 60 HZ input power.

The power supply as proposed allows for only one memory cartridge at a time to be active, while the remaining memory cartridges are in standby. "Active" meaning that the cartridge is being accessed, read, or written.

The Mass Storage Subsystem (MSS) proposed is a non-volatile bubble memory which will store data permanently or may be rewritten, as desired. The subsystem, shown in Figure 2.2-1, is exactly the same as that provided for the MX Peacekeeper C^3 program except that it is extended to include two I/O ports rather than one, and four removable memory cartridges, rather than one memory cartridge.

All off-the-shelf subassemblies (Bubble Memory cards, microprocessor card, RAM/ROM card, and I/O cards) are shown functionally in Figure 2.2-1. The only new design is a "Buffer Card", consisting of special logic components, which allows for the previously described extension of off-the-shelf components (2 ports, and 4 memory cartridges) shown functionally in Figure 2.2-1. The functions depicted are fully in accordance with the requirements specified in paragraph 3.1 of MSS Specification CS-GSK-002, dated 16 January 1985.

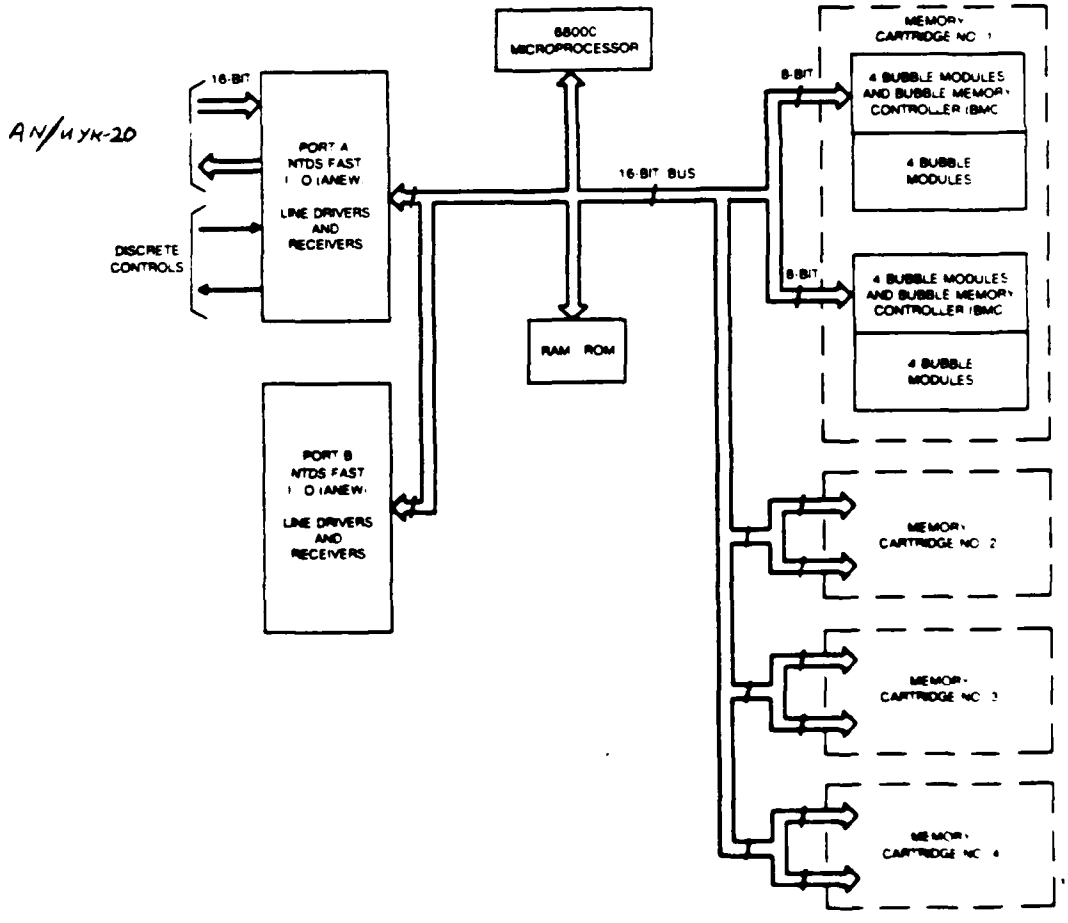
Photographs of the existing design QuadI/Quad II Bubble Memory cards, Microprocessor card, RAM/ROM card, and I/O card are shown in Figures 2.2-2 through 2.2-5, respectively.

Two I/O ports per MIL-STD-1397 Type C (ANEW) are provided to interface the AN/UYK-20. These ports (Port A and Port B) are available on a first come-first serve basis to each host. Instantaneous data transfer rates are up to 100 kHz per word (16-bit word) and up to 68 kHz effective word rate, considering overhead. (See Statement of Work Compliance to Specification, para. 3-1.2.1.)

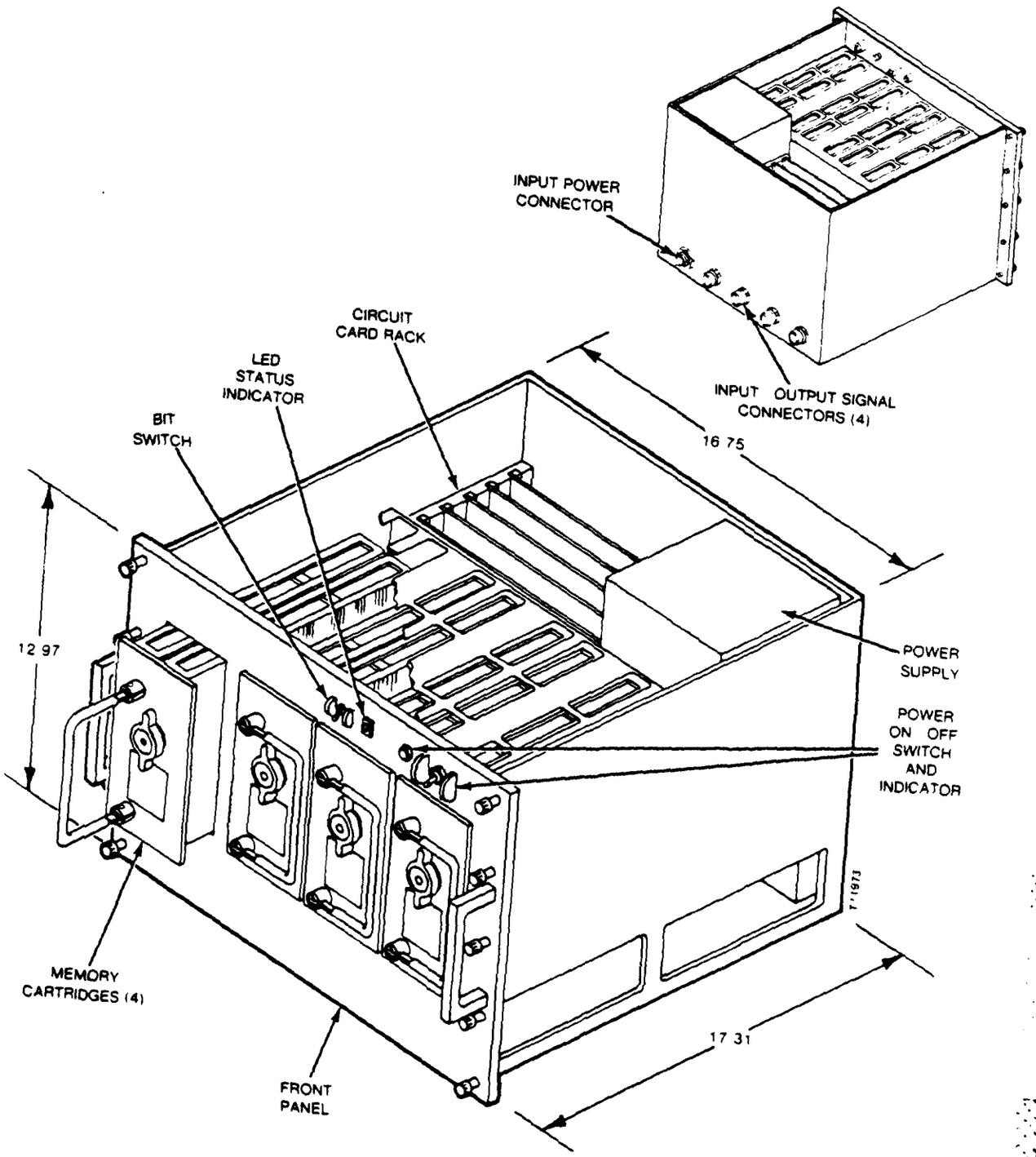
Each of the four removable memory cartridges contains 1,048,576 words of usable data (16-bit words). Sixteen bubble modules divided into two sets of eight, each set with its support chips and one Bubble Memory Controller (BMC), constitute this non-volatile storage. Only one memory cartridge is active at any one time, thus 16 bubbles, two BMC's (each with an 8-bit bus), are active while all other memory cartridges are in the standby mode. The bus at the memory cartridge interface is an effective 16-bit bus as are, notably, all of the bussing within the subsystem.

The Motorola 68000 is a basic microprocessor utilized throughout Librascope supplied equipment. In the proposed MSS, it functions as the transparent controller providing DMA transfers between the memory cartridges to RAM, and RAM to I/O. Most importantly the microprocessor provides the emulation of the Command Word instructions from the host and the development of the emulated Status Word to represent that required from the inherent function of the bubble memory.

Also residing in firmware will be BIT (Built-in-Test), which will be performed upon power-up, after a power fail, after insertion of a memory cartridge, and upon manual initialization. Initialization (reset) will always include BIT.

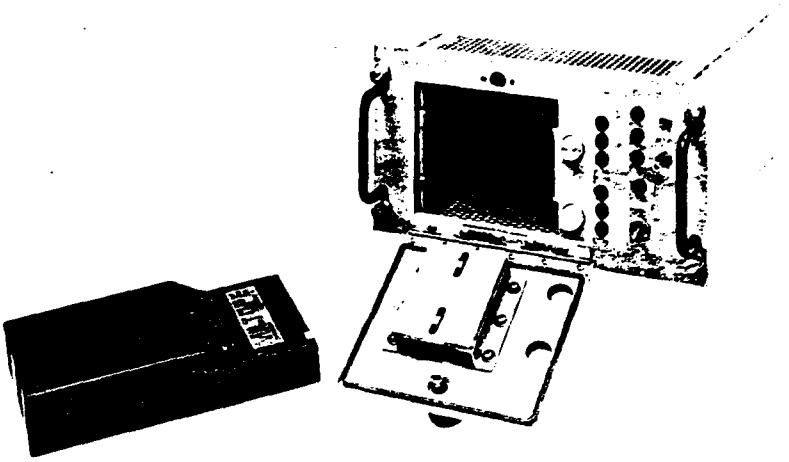


Bubble Memory System Block Diagram



Mass Storage Subsystem Proposed Design Approach

BMS-1000 BUBBLE MEMORY SUB-SYSTEM



BMS-1000 Bubble Memory Sub-System

FEATURES:

- Removable Bubble Memory Cassette
- 128K Byte or 256K Byte Storage Capacity per Cassette
- Total 'On-Line' emulation of Industry Standard 'Floppy' disk subsystems
- Compliance to MIL-E-16400/ MIL-E-5400/MIL-E-4158
- Rugged Cassettes Withstand 60G Shock
- Non-Volatile Storage – Power Loss Data Protection
- Automatic Error Correction
- Memory Write Proection
- Low Power Consumption

DESCRIPTION

Miltope's BMS-1000 Bubble Memory Sub-system is a solid-state, on-line random access memory that functionally emulates industry standard flexible disk drives. The subsystem, physically interchangeable with existing militarized 'floppy' diskette drives, serves to eliminate the electro-mechanical complexity associated with diskette drives, thereby reducing the need for highly trained technicians and greatly enhancing system uptime.

BMD BUBBLE MEMORY DRIVE

The bubble memory drive contains holders for two cassettes, along with a power supply and a formatter configured to emulate an RX01 interface to a Norden PDP-11M or DEC PDP-11 type computer. Computer drive software will operate the bubble memory sub-system as if it were a diskette, thus enabling integration of the bubble memory without operating system software changes.

Since the overall dimensions of the rugged aluminum drive housing are identical to Miltope's 8-inch flexible disk drive, physical as well as functional interchangeability is assured.

The front panel of the drive contains a control panel and an RFI gasketed access door. The access door protects two openings that accept any combination of single-bubble (128K byte) or double-bubble (256K byte) cassettes. A cassette locking knob adjacent to each opening secures the cassette and causes power to be applied. Conversely, unlocking the knob provides a controlled power-down to assure that no extraneous signals are transferred to the cassette during its removal from the drive housing.

Each cassette holder in the drive enclosure functions as the equivalent of a disk drive unit.

Special attention has been directed towards assuring memory system compatibility between Intel's Plug-a-Bubble™ and Miltope's BMS-1000. Within storage capacity limits, either the Miltope cassette or Intel's Plug-a-Bubble™ (with Miltope adapter) can be inserted into the BMD-102 drive for 'on-line' operation without configuration changes.

BMC BUBBLE MEMORY CASSETTE

The BMC Bubble Memory Cassette contains 1 or 2 memory modules plus associated control electronics. Each cassette provides 128K bytes (BMC-128) or 256K bytes (BMC-256) of storage with the 1 megabit module.

The 256K byte module contains sufficient storage to emulate a single-sided single-density 8-inch diskette. The bubble cassettes are designed for ease of removal and replacement within the system as simply as 'floppy' disk media are removed and replaced within flexible disk drives.

A spring-loaded connector cover automatically seals the cassette against sand, dust, water, and other adverse elements whenever the cassette is not inserted in the drive. Each cassette includes a write protect actuator to assure data integrity and contains internal buffering electronics that isolate sensitive low-level signals from the interface.

SYSTEM POWER

Standard primary power to the drive unit is 115/220 volts, 47-440Hz, single phase. This power services most airborne and shipboard applications. Optional 28VDC (nominal) input is available for vehicular applications. EMI filtering is provided to prevent line transients from affecting memory operation, as well as to meet the noise restrictions associated with military equipment.

SPECIFICATIONS

DRIVE (including cassettes)

Emulation	DEC RX01 Single Sided/Single Density emulation of 2-drive 'floppy' system
Capacity	512K bytes
Transfer	*Buffered storage on BMS-1000 provides same thru-put as 'floppy' sub-system.*
Physical size (chassis)	Height: 5.0" Width: 8.44" Depth: 14.4"
Weight (excluding cassettes)	15 pounds
Vibration	MIL-E-5400 - amplitudes to 5G's, 5 to 2000Hz
Shock	40G's, 1/2 sine, 11ms
Temperature	
operating	-18°C to +55°C
non-operating with data retention	-40°C to +100°C
Humidity	95% RH
Altitude	
operating	50,000 ft

EMI	Per selected requirements of MIL-STD-451
Fungus	Per MIL-STD-810
Salt atmosphere	Per MIL-STD-810
Sand & dust	Per MIL-STD-810
Data reliability	With error correct 1 in 10^{15}; W/O error correct 1 in 10^{9}
Power	115/220 volts ± 10%, 47 to 440Hz, single phase
optional	28VDC
Power consumption	70 watts

BUBBLE CASSETTE

	BMC-128	BMC-256
Capacity (formatted)	128K bytes	256K bytes
Transfer rate	12.5K bytes/second	25K bytes/second
Access time (average)	48ms	48ms
(maximum)	96ms	96ms
Shock	60 G's, 1/2 sine 11 ms	60 G's, 1/2 sine 11ms
Vibration	MIL-E-5400 Amplitudes to 10G; 5 to 2000Hz	MIL-E-5400 Amplitudes to 10G; 5 to 2000Hz
Water immersion	3 ft. per MIL-STD-108	3 ft. per MIL-STD-108
Temperature		
Operating	-18°C to +55°C	-18°C to +55°C
Non-operating with data retention	-40°C to +100°C	-40°C to +100°C
Altitude	50,000 ft.	50,000 ft.
Humidity	100% RH	100% RH
Fungus	Per MIL-STD-810	Per MIL-STD-810
Salt atmosphere	Per MIL-STD-810	Per MIL-STD-810
Sand & dust	Per MIL-STD-810	Per MIL-STD-810
Drop test	36" drop	36" drop
Size	4.0"x8.0"x1.19"	4.0"x8.0"x1.75"
Weight	28 oz.	36 oz.

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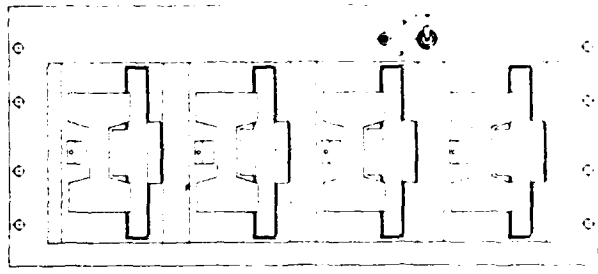
BDS-5R SERIES

Bernoulli Disk Drive Systems
Ruggedized

MILTOPE
CORPORATION

FEATURES

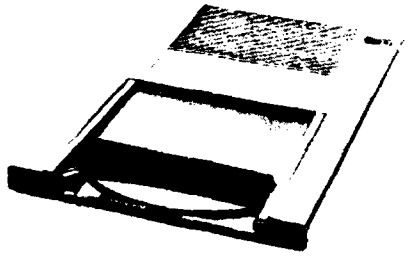
- Bernoulli Flexible Disk Cartridge Technology
- Easily removable, low cost 5-1/4 inch disk cartridge
- Absolute cartridge interchangeability from drive to drive
- Large storage capacity of 5 megabytes per cartridge
- Fast data transfer rate of 5 megabits per second
- Fast data access time of 40 milliseconds average
- Extensive data error detection and correction for greater data reliability
- Highly resistant to shock and vibration - no "head crashes"
- Small physical size
- Designed for rugged environments



BDS-504R Bernoulli Disk System

DESCRIPTION

The Miltope BDS-5 Series of mass storage systems contain high capacity, high performance, low-cost, flexible media cartridge disk drives utilizing Bernoulli Disk Technology.
The magnetic medium is a 3-mil thick, 5-1/4 inch mylar flexible disk. This disk is housed in a cartridge which closes when removed from the drive to protect it while being handled. When the cartridge is inserted into the drive, the disk is exposed to a flat plate and read-write head over which it will fly. This disk is magnetically coupled to the drive motor and as it spins close to the flat plate and read-write head, the disk stabilizes and flys at a very small distance above the plate and head. This technology offers high storage capacity, fast access, and fast data transfer while using low-cost removable cartridges. Absolute cartridge interchangeability is achieved by a track-following, closed-loop servo system. A rotary voice coil actuator "coarsely" positions the head to the required position, the servo system "finely" positions the head to the exact track position, and then the servo system keeps the head in this exact position until a different track is required.



BETA-5 Bernoulli Disk Cartridge

BDS-5R SERIES CAPACITIES

The BDS-5 Series of systems offer various storage capacities as shown in Table I. The standard electrical interfaces are ST-506 or SCSI. Various interfaces can be provided for NTDS, Unibus, 1553B, and others.

Specifications

CAPACITY

USER AVAILABLE (FORMATTED) CAPACITY, BYTES

BDS-501R	5,244,928
BDS-502R	10,489,856
BDS-504R	20,979,712
Cartridge (BETA-5™)	5,244,928
Surface	5,244,928
Track	13,312
Sector	256

BYTES PER FORMATTED CARTRIDGE

User Available	5,244,928
Spare Capacity	
. For Factory Flagging, Max.	403,456
Overhead	1,875,440

ORGANIZATION

CONFIGURATION

Cartridges Per Drive	1
Flexible Disks Per Cartridge	1
Recording Surfaces Per Flexible Disk	1
Formatted (user-available) Tracks Per Surface	394
Formatted (user-available) Sectors Per Track	52
Bytes Per Record	256

PERFORMANCE

DATA TRANSFER RATE ..... 5.0 Mbits/sec

SEEK TIME (a)

Minimum	6 msec
Average	39 msec
Maximum	87 msec

SETTLING TIME

Single Track	5 msec
Maximum	11 msec

LATENCY (average rotational delay) ..... 15.3 msec

Spindle Speed ..... 1,964 rpm

START/STOP TIME (average) ..... 10/5 msec

Table I
BDS-5R Series
Mass Storage Systems

Storage System	Number of Drives	Storage Capacity	Physical w" x h" x d"
BDS-501R	1	5Mbytes	8-1/2 x 9-3/8 x 11-3/4, 20 lbs
BDS-502R	2	10Mbytes	10-1/2 x 8-3/4 x 19-5/8, 40 lbs
BDS-504R	4	20Mbytes	19 x 8-3/4 x 19-5/8, 60 lbs

ENVIRONMENT

OPERATING

Temperature	+5°C to +46°C
Relative Humidity (noncondensing)	10 to 80%
Altitude	10,000 ft
Shock (b)	15 G's for 11 ms, half sine wave
Vibration (b)	.075 DA to 2.5 G's to 2000 Hz

RELIABILITY

ERROR RATES

Data	
. Soft	$<1:10^{10}$ bits read
. Hard	$<1:10^{12}$ bits read
Seek	$<1:10^{6}$ bits read

MEAN TIME BETWEEN FAILURES

Drive ..... >10,000 POH

MEAN TIME TO REPAIR ..... 0.5 hrs

SERVICE LIFE ..... 5 years

CARTRIDGE INSERTION/REMOVAL CYCLES,

Minimum (design life) 10,000

a) Does not include step pulse transfer time
b) Each specified shock and vibration level is applied separately to each of the three mutually perpendicular planes of the drive; the planes being defined as the top, front, and side

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APPENDIX B

DISPLAY AND CONTROL CONSOLE INFORMATION

(EXCERPTED FROM NAVELEX EE150-BV-MMO-010(C))

3-64(U). DISPLAY AND CONTROL CONSOLE (DCC) — 5A2.(U) The DCC is the control center of the countermeasures set. Symbolic data in graphic form or alphanumeric information is displayed on the display monitor. Also, various audio/visual alert information is indicated. Operator inputs are generated by use of various switches, controls, and a typewriter keyboard. Built-in test (BIT) indicators designate certain malfunctions that are detected by the system operability and diagnostic tests. The test information is displayed in alphanumeric format on the display monitor.

The DCC consists of the operator display and control console (ODCC) and the cartridge tape transport (CTT). There are three subsystems in the ODCC: the operator interface subsystem, the display subsystem, and the display data processing unit (DDPU) subsystem. The overall DCC, according to this organization, is shown in figure 3-78. The majority of the DCC circuits is within the ODCC. The CTT is a mass storage unit; it holds the operational and system diagnostic programs. Information is transferred as serial digital data between the CTT and the DCC and between the CTT and the DPU, the latter by way of the ODCC. Data transfers and control information are exchanged between the three subsystems by way of a bidirectional bus. Refer to Volume IV, figures 5-BD805001 and 5-BD805002 for block diagrams of the CTT and the ODCC, respectively. The interface and data transfers between the DCC and the DPU are covered in paragraphs 3-21 through 3-24. Refer to these paragraphs for the following descriptions.

3-21 — Program load processing

3-22 — Keyboard to computer and console processing

3-23 — FAB to computer and control processing

3-24 — DPU to console display processing.

a(U). Operator interface subsystem.(U) This subsystem is shown in figure 3-79 including the display monitor (part of refresh/display subsystem). The operator interfaces with the DCC and other parts of the countermeasures set via controls, lamps, switches, audio alerts/alarms, and associated circuits in this subsystem. The controls interface is the interface between this subsystem and the DDPU, by which the interface is further extended to the DPU. Additional interfacing includes power, control signals, audio for both speaker (alarms/alerts audio) and headset (voice communication's audio), and chaff launcher control and status signals as shown on figure 3-79.

(1)(U) Controls interface - 5A2A5A9 (U) This circuit card controls and processes data transferred between the DDPU and the operator interface subsystem. The data is transferred under program control A0 or from the following peripherals: shelf operator keyboard, shelf operator pushbuttons, switches, lamps, stiff stick and chaff launcher interfaces; overhead module; and auxiliary panel. Data transferred between the DDPU and the controls interface is in parallel format. Data from the overhead module, the

Table 3-185 (U). Synchro/Digital Data Format (U)

Device Code	I/O mode	Function	Synchro position	Digital output (LSB) resolution
40_4	DIA	Ships heading	0° to 360°	360/1024 degrees = 0.35°
40_5	DIC	Ships roll	0° to 180°	180/1024 degrees = 0.18°
41_5	DIA	Relative wind speed	0 to 100 knots	1000/1024 knots = 0.098 knots
41_6	DIC	Relative wind direction	0° to 360°	360/1024 = 0.35°

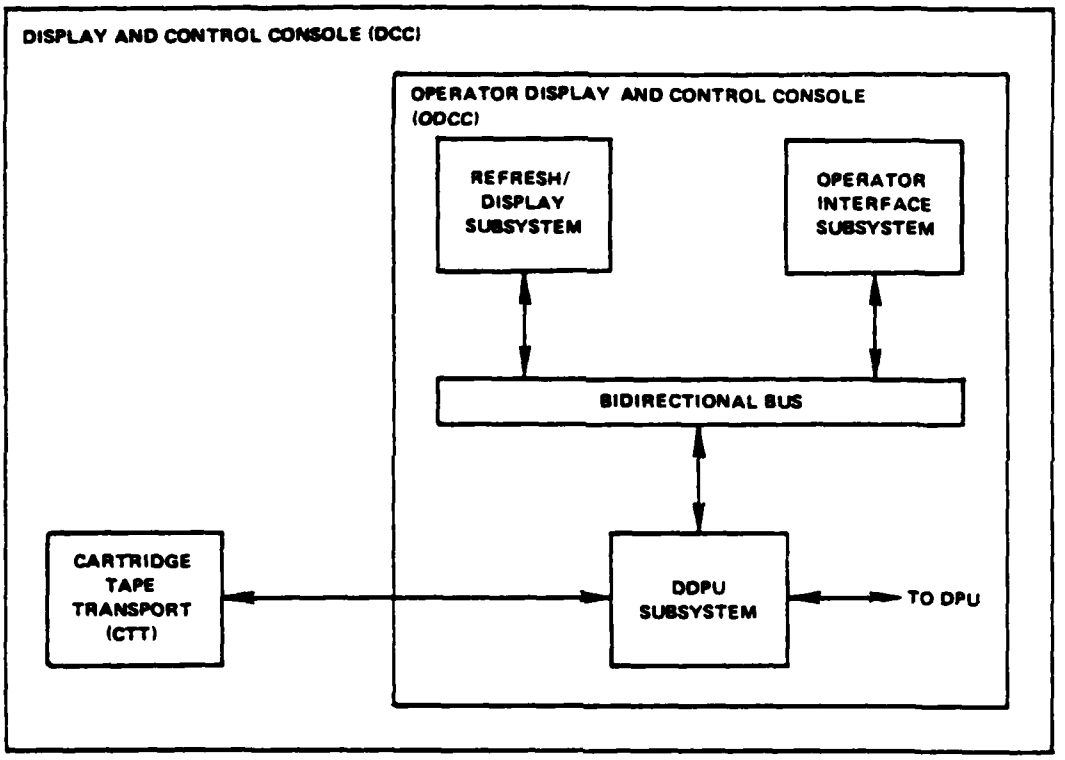


Figure 3-78 (U). General Organization of Operator Display and Control Console (ODCC) (U)

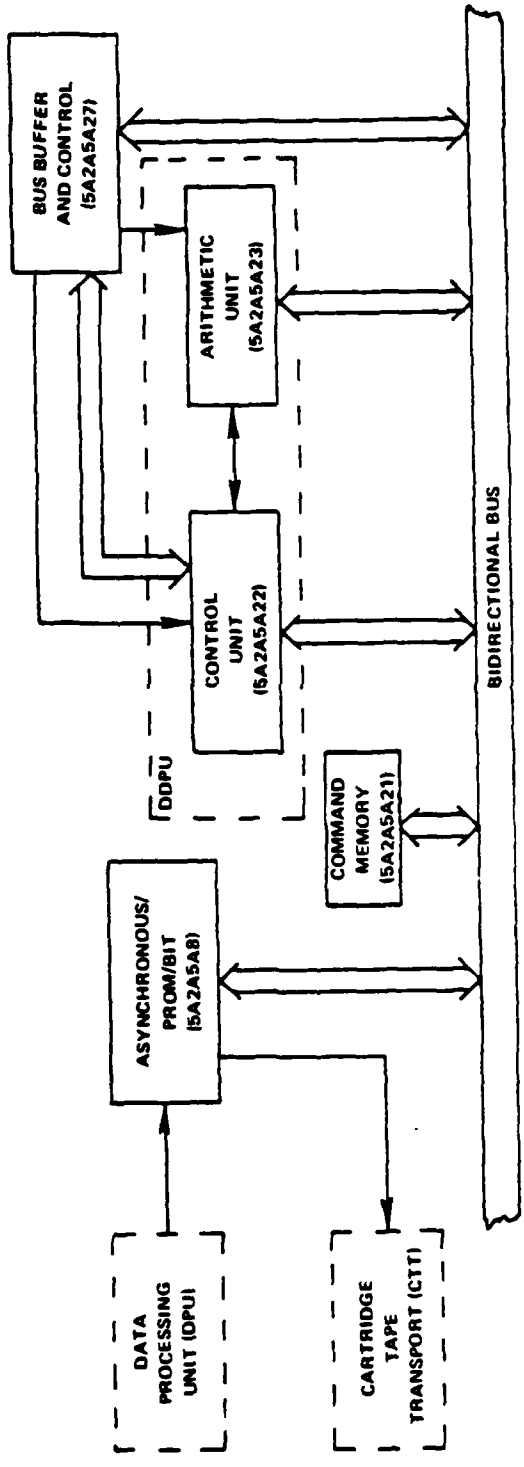


Figure 3-81 (U). DDPU Subsystem (U)

displayed only at one intensity, as opposed to the bright or normal video display characteristics of the alphanumeric and symbol generator display video. The dot memory is an integral part of the dot generator circuit card.

(5)(U). Format (circle) generator — 5A2A5A11 (U) The format generator produces the video that is used to display a polar format on the CRT. The alphanumeric, symbol, and dot video displayed within the three concentric circles of the polar format are produced by their respective generators, thus providing information for the operator to track and identify surface and subsurface vessels and aircraft within the environmental area that is being displayed. When the polar format is displayed, the circles are offset to the upper right on the CRT to allow presentation of tabular data in the corner margins of the screen. The format generator stores data words and repeat bits in its PROM, and outputs this combined information for each unique scan line. This per-line process is repeated until the entire polar format is displayed; it is maintained through refreshment techniques. All video displayed on the CRT is refreshed at the rate of 50 times per second.

(6)(U). Timing generator — 5A2A5A10.(U) The timing generator receives digital video signals from the various DCC video generators, performs digital-to-analog conversion, and outputs mixed video to display monitor 5A2A2. The timing generator also outputs several timing and control signals for synchronization of the DCC video generators and the display monitor. The basic clock signals are provided by an oscillator in the timing generator. Other clock and timing signals are multiples of the basic clock. Signals produced in the timing generator circuits associated with the digital-to-analog conversion synchronize the output of analog video with the scanning beam position on the display monitor.

(7)(U). Display monitor — 5A2A2.(U) The display monitor consists of four SRAs: the power module 5A2A2A1, the deflection module 5A2A2A2, the video module 5A2A2A3, and the CRT assembly 5A2A2A4. Functioning together, these modules provide for the display of information to the operator from all the video generators in the DCC, providing symbolic information of the environment surrounding the home ship in graphic format and alphanumeric printouts. In addition, data and information resulting from system testing, both resident systems operability tests (SOT) and tape-loaded DSIs are displayed on the CRT as alphanumeric characters.

(a)(U). Power module — 5A2A2A1.(U) The power module is a circuit card assembly that contains a power module and the associated circuits necessary to provide power for the display monitor assembly. It supplies the CRT anode, focus, and intensity voltages as well as the filament heater power and DC voltage for the video and deflection modules.

(b)(U). Deflection module — 5A2A2A2.(U) The deflection module contains circuits which perform horizontal and vertical deflection of the electron beam to the CRT, generating a 720-element by 576-line raster display. Synchronization signals are received from the timing generator 5A2A5A10.

(c)(U). Video module — 5A2A2A3 (U) The video module contains circuits which receive low-level video signal information and modulate the electron beam in the CRT for the visual display.

(d)(U). CRT assembly — 5A2A2A4.(U) The CRT assembly consists of a 10" by 12" CRT, a deflection yoke, and a connector cable. The usable surface area of the CRT, when in operation, is 8" by 10". The CRT operates in a non-interlaced mode.

Display monitor 5A2A2 has operator-adjustable controls for contrast and brightness and an interlock safety switch which automatically shuts off the horizontal drive voltage to the CRT whenever the monitor drawer is opened. Test points for troubleshooting and a series of LEDs for indication of proper circuit operation also are provided.

c(U). DDPU subsystem.(U) This subsystem includes five circuit cards as shown in figure 3-81. Also shown in this figure are the DPU and the CTT because their functions are closely related to the DDPU and the other two ODCC subsystems, operator interface and refresh/display. The central function of this subsystem is the DDPU. This unit contains two closely interrelated circuit cards, the control unit and the arithmetic unit. The DDPU is a microprocessor whose main function is to control the various data transfers between all DCC functional units connected to the DDPU bidirectional bus, the DPU, and the CTT. The command memory is DDPU-dedicated and provides storage for computer programs and data utilized by the DDPU. The bus buffer and control functions primarily for initiating the DCC startup and reset operations. The asynchronous interface/PROM/BIT circuit card ACIA accomplishes the following: interfaces the DDPU with the DPU and the CTT, acts as the repository for bootstrap-loading and startup test programs (resident in PROM on this circuit card), and decodes and displays BIT information related to tests conducted during DCC startup and program loading from the CTT.

Communications between the DDPU and DPU or the CTT are by serial data transmissions, whereas, within the DCC, the DDPU communications are by parallel data transmissions by way of a bidirectional bus (which is the same bus shown on figures 3-79 and 3-80 for the operator interface and refresh/display subsystems). All such communications are initiated and conducted under program control.

(1)(U). DDPU – 5A2A5A22 and 5A2A5A23 (U) The DDPU control unit decodes instructions and, based on the results, addresses a microroutine (in the control unit). The microinstructions of the microroutine produce various control words and signals that implement the instruction. Certain control signals are transmitted to the arithmetic unit, which contains several registers and an arithmetic/logic unit. The appropriate data are manipulated (in the arithmetic unit) by the control signals to perform arithmetic, logic, and data transfer operations.

During startup/reset, an address, generated in the bus buffer, is received by the control unit. This address points to the location of the DCC initialization routine. The DDPU accesses this address, and turns over control to the startup/loader program in the PROMs of the ACIA circuit card.

After the DDPU is initialized, its operations are controlled by programmed input/output software. During these operations, the DDPU is the master and all other units to which it interfaces are slaves. These slaves are called peripherals; they include the DPU, CTT, and all operator interface and refresh/display functional units connected to the DDPU bidirectional bus.

(2)(U). Bus buffer and control – 5A2A5A27 (U) This circuit card includes two types of circuits, the startup sequencer and extended bus circuit. In the operation of the DCC as part of the overall countermeasures operations, the extended bus circuit has only a minor function: indication of the status of certain controls signals and addresses, both connected to their respective lines of the bidirectional bus. These indicators are useful primarily for troubleshooting.

The startup sequencer circuit is used only when the DCC is initialized. When power is turned on by the system power switch or by pressing and releasing the PRGM LOAD switch on the overhead panel, a reset/restart operation is initiated. Various peripherals are reset and operation of the DDPU is initiated by a particular new startup address sent by the bus buffer and control to the DDPU. This address directs control to the program in the PROM in the ACIA circuit card.

(3)(U). Asynchronous/PROM/BIT – 5A2A5A8 (U) This circuit card has three discrete but interrelated functions. They are the asynchronous interface adapter (ACI) for handling data transfers between the DDPU and both the DPU and the CTT; the bootstrap loader for loading programs from PROM (on this card) during restart of the DDPU; and BIT indicators for displaying BIT results obtained as a consequence of tests conducted in conjunction with bootstrap loading.

(a)(U). ACIA (U) The ACIA communicates with the CTT or the DPU by serial data transfers, but with the DDPU by parallel data transfers via the DDPU bidirectional bus. There is no direct communications path between the CTT and the DPU. To transfer data between these units, the data is routed from either the CTT or the DPU through the ACIA to the DDPU. The data is routed back through the ACIA to either the DPU or CTT, as appropriate. Thus, the following data transfers are processed: CTT to/from DDPU; DPU to/from DDPU, and CTT to/from DPU.

(b)(U). Bootstrap PROM (U) During a restart sequence, the DDPU addresses the bootstrap PROM. The contents of the PROM are loaded into the DDPU command memory. These contents include a loader program, DCC and DCC – interface test routine, and the CP-32 utility program.

(c)(U). BIT INDICATORS (U) During startup/reinitialization of the DCC, 10 BIT indicators on the edge of the ACIA cards are set (extinguished) and lit in consecutive order while the various initialization tests are conducted. A particular indicator lights upon commencement of the corresponding test and is extinguished if the test is completed successfully. If the test is not so completed, the light remains lit and the reinitialization is aborted. Indicator lights are lighted and extinguished in order, providing tests are completed without faults, until the entire sequence of tests is completed. More details and the significance of these indicators are given in Section XI of this chapter.

(4)(U). Command memory – 5A2A5A21 (U) This memory circuit card is a 4096-word by 16-bit dual-port, RAM. It is dedicated to the DDPU and is used for storage of computer programs and data. This RAM is connected to the DDPU bidirectional bus.

SECTION XXI(U). DISPLAY AND CONTROL CONSOLE (DCC).(U)

3-279(U). INTRODUCTION.(U) The display and control console (DCC) comprises two major assemblies, cartridge tape transport (CTT) 5A1 and DCC 5A2. The operational systems computer programs (software) system diagnostic tests and on-line libraries are resident on magnetic tape cartridges. These software items transferred from the CTT to the DCC are used therein, and are also used elsewhere in the system. The CTT may also be used for transferring software from the DCC to magnetic tape. The ODCC comprises the remainder of the DCC and provides the means for operator interface with the countermeasures set.

The CTT is described under the heading Cartridge Tape Transport, immediately following this introduction. An overview of the DCC, described next, generally interrelates functions performed by the many circuit cards, other types of modules, and control panels that comprise the DCC under the heading of Display and Control Console.

More detailed functional descriptions of the circuit cards, other modules, and the control panels follow. These descriptions are oriented to a circuit card level of explanation. As such, their main purpose is to support troubleshooting at the circuit card level.

3-280(U). CARTRIDGE TAPE TRANSPORT — 5A1.(U) The CTT (figure 3-117) is a mass data storage peripheral unit used for loading operational programs, system diagnostic test programs (SDTs), and a prerecorded online library into the digital processor unit (DPU) and digital display processor unit (DDPU). The data is stored on a DC300 1/4" tape cartridge utilizing four tracks recorded serially. The CTT consists of four circuit cards: tape transport drive A2, tape transport interface circuit card assembly A1, low voltage power supply PS1, and fan blower B1.

a.(U). Tape transport drive — 5A1A2.(U) The tape drive records and writes phase encoded digital data serially on four tracks of a tape cartridge cassette. The tape drive operates at 30 inches per second (ips) during tape read or write operation and at 90 ips during search, rewind, and fast forward operation with a recording density of 1600 bits per inch (bpi).

The primary elements of the drive are the magnetic bead, the sensor assembly, the data board, the servo board, the interconnect board, the motor mount assembly, and the basic mechanical assembly to which all of the above are attached.

The tape drive receives power from low voltage power supply (LVPS) 5A1PS1 via wire harness connector P2, which mates with connector J1 of the tape drive (figure 3-117). The power requirements are +5 VDC, +28 VDC and −28 VDC. The remaining tape drive signals interface directly with tape transport interface CCA 5A1A1. These interface signals can be classified into five categories. They are the unit address/select signals, the tape motion control signals, the track select signals, the data signals, and the drive status signals. A functional description of each signal in its respective category follows.

(1)(U). Unit address/select signals.(U) The unit address/select signals consist of drive input signals SL1− and SL2−. These signals are used for device codes in multiple drive systems to select a particular drive. Tape transport assembly 5A1 has only one drive; thus, the SL1− and SL2− drive inputs are tied to the same output (SEL1−) from the tape transport interface card.

The drive will not respond to the tape motion control signals, the data signals, or the track select signals unless the SL1− and SL2− input signals are in the logic LOW state.

(2)(U). Tape motion control signals.(U) The tape motion control signals consist of the following active low drive inputs.

HSP- In the logic LOW state, this signal causes the tape to move at high speed (90 ips) in the direction set by the FWD− or the REV− signals. In the logic HIGH state, this signal causes the tape to move at the nominal speed of 30

FWD- In the logic LOW state, this signal causes the tape to move in the forward direction.

REV- In the logic LOW state, this signal causes the tape to move in the reverse direction.

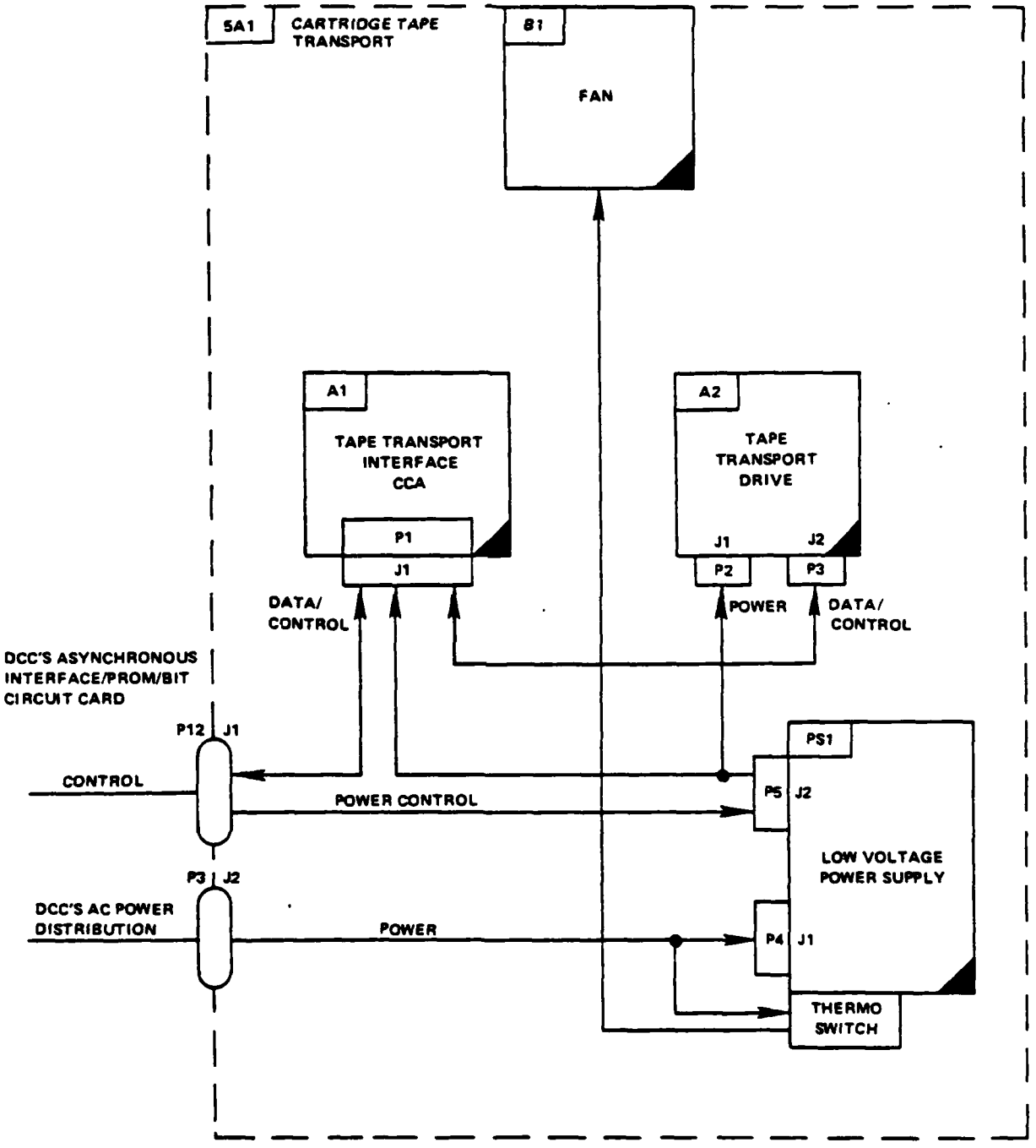


Figure 3-117 (U). Cartridge Tape Transport Simplified Block Diagram (U)

If, by accident, both the FWD− and REV− signals are in the logic LOW state simultaneously, circuitry in tape drive will stop the tape motion. To stop the tape motion, the tape transport interface card conditions the FWD− and REV− signals to a logic HIGH.

(3)(U). Track select signals.(U) The track select signals include the TR1 and TR2 input signals. The tape transport interface card selects one of four tracks by conditioning the TR1 and TR2 signals, as shown below.

TRACK no.	TR2	TR1
1	L	H
2	H	L
3	H	H
4	L	L

(4)(U). Data signals.(U) The data signals consist of five signals, including the ERA−, NDA−, WEN−, and HIT− input signals and the RDA− output signal. A description of each signal follows.

ERA− When LOW, this signal enables or turns on the tape erase function (erase head) for the track selected by TR1 and TR2.

WDA− This WRITE DATA signal is the input used to modulate the unit head to record data on tape when the WEN− signal is LOW.

WEN− To enable writing (recording) on tape, this WRITE ENABLE signal must be LOW. Writing will continue until this signal goes false. The writing function is disabled by circuitry in the drive if the cartridge is write-protected.

HIT− When LOW, this signal raises the read detection threshold to 50%, of the nominal maximum of the read signal from the read head. The LOW threshold is nominally 20%. The HIGH threshold (HIT− is true) is used during high-speed searching and during read-while-writing to improve noise immunity. During read-while-write operation, the higher threshold also ensures that a strong recording has been made on the tape.

RDA− The READ DATA is the output signal of the drive used to recover the data on the tape during tape read operation. This signal is a replica of the WDA− data written on tape.

(5)(U) Drive status signals.(U) The tape drive contains sensors that provide five drive status output signals. These signals include the cartridge in place (CIP+), the file unprotected (FUP+), the bulb (BLB−), the upper light sensor (ULS−), and the lower light sensor (LLS−) signals. A description of each signal follows.

CIP+ When HIGH, this signal indicates that a tape cartridge is installed on the drive. The sensor for this signal consists of a switch that is activated when the cartridge is installed. The tape transport interface CCA monitors this signal to verify that a cartridge is in place before issuing any drive motion commands.

FUP+ When HIGH, this signal indicates that the tape cartridge is not write-protected. The sensor for this signal consists of a switch that is or is not activated, depending on the position of the tape cartridge safety, when the cartridge is installed on the drive. The switch is activated when the safety arrow points away from SAFE. The tape transport interface CCA monitors this signal to determine if the cartridge or file is unprotected. The tape transport interface CCA will not attempt to record data on tape if the cartridge is write protected. (Safety arrow on SAFE or FUP+ is LOW.)

BLB− The tape drive contains a light source that acts as a stimulus for two light sensors. The light source consists of a light bulb that is lit when power is applied to the drive. When LOW, BLB− indicates that the light bulb is on and drawing current. The tape transport interface CCA monitors this signal to verify that the bulb is not burned out. If the BLB− signal is HIGH, the tape transport interface CCA will not initiate any tape drive operation.

ULS− When LOW, this signal indicates that a tape hole has been detected in the upper half of the tape.

LLS− When LOW, this signal indicates that a tape hole has been detected in the lower half of the tape.

The tape cartridges that are used with the tape transport assembly have holes located at the beginning of tape (BOT) and at the end of tape (EOT), as shown in figure 3-118. Some of the holes are located in the upper half (track 2 and 3 area) of the tape, and some in the lower half (track 1 and 4 area).

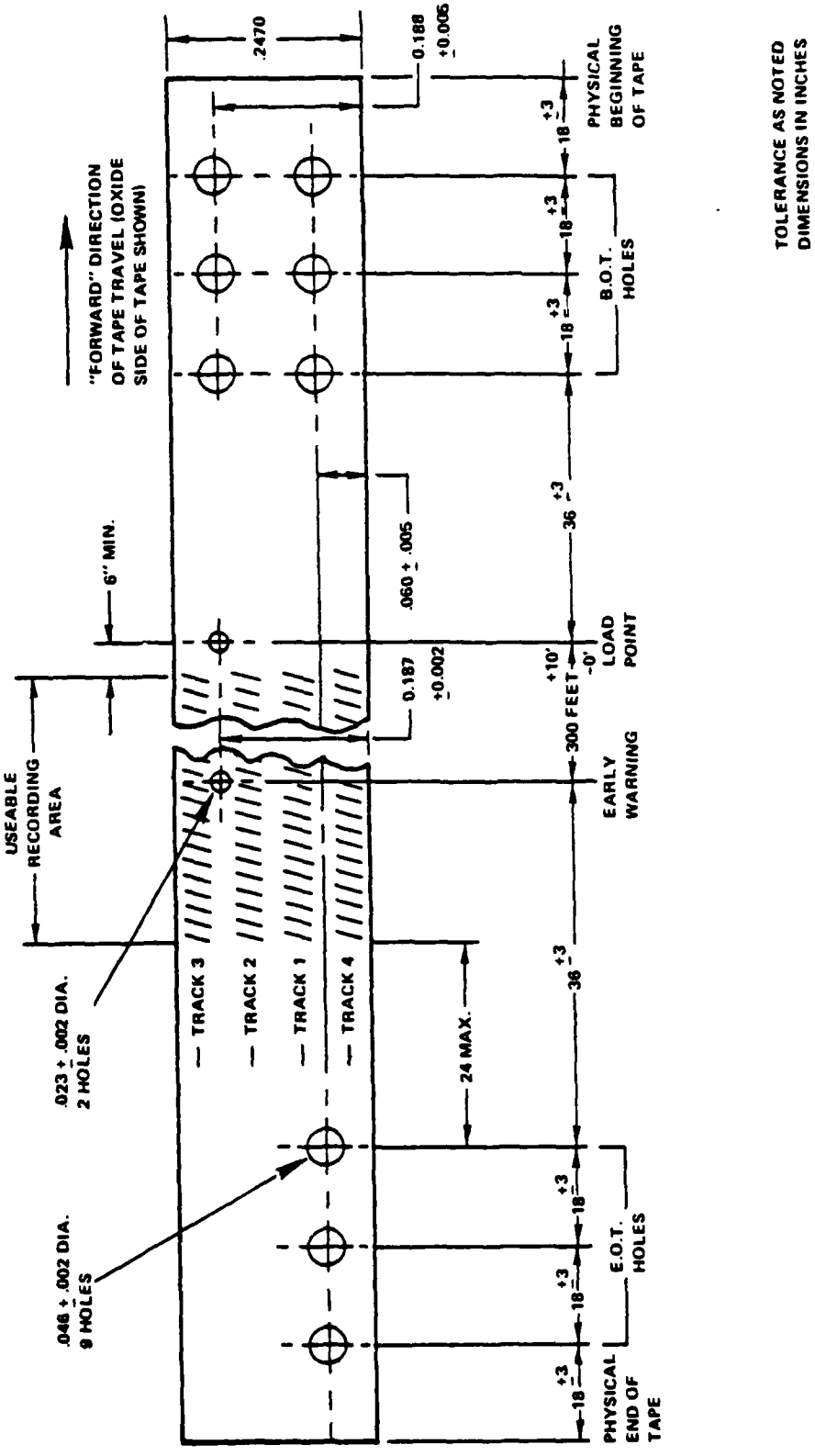


Figure 3-118 (U). Tape Position Holes and Recording Format (U)

The tape transport interface CCA monitors the ULS− and LLS− signals while the tape is in motion to determine when BOT or EOT is reached. When holes are encountered, it interprets the pattern of the hole sensed to determine if they are BOT or EOT holes.

b(U). Tape transport interface — 5A1A1.(U)
The tape transport interface circuit card assembly is a controller interface that provides a single-channel asynchronous interface for bidirectional communication with the cartridge tape drive, and functions as an input/output (I/O) device between the system and asynchronous interface/PROM/BIT circuit card assembly 5A2A5A8 to the DDPU and DPU.

The central processor unit chip (CPU) on the tape drive interface is a microprocessor that controls the interface between the serial I/O ports and the tape transport drive. This CPU is supported by a read only memory (ROM) for its firmware program, two 1024-by-4-bit static random access memories (RAMs) and an 8 Mhz clock oscillator circuit, which also provides clock timing for the synchronous serial data adapter (SSDA), the asynchronous communications interface adapter (ACIA), and counter circuits. This clock is divided down and processed through select circuits to be used by the other circuits. A 12-bit address bus from the CPU interconnects with its support circuits such as the ROM, RAM, SELECT CKT, DRIVE STATUS DATA REGISTERS, ACIA, and SSDA. All data and command words sent across the DCC/tape channel have a serial data bit length of eight bits, and each data path is functionally terminated and controlled by an ACIA. The ACIA and the SSDA convert parallel data to serial data (and serial data to parallel data) for communication between units. They act as an output latch for the eight parallel bits being sent out, and as a holding register for the serial data being received. The SSDA interfaces the CPU data lines with control I/O signals WEN−, WDA−, and RDA− from the tape drive. The ACIA serves as an interface for the data and command words sent across the DCC/tape channel after going through line receivers or line drives.

The following input signal pairs are buffered through balanced line receivers (LINE RCVR): suffix H = high and L = low.

Input pairs	RQCXL RQCXH	Serial clock
	RQDIL RQDIH	Serial data
	RQSTRL RQSTRH	Start

The following output signal pairs are buffered through line drivers: suffix H = high and L = low.

Output pairs	QPWRL QPWRH	Tape drive power
	QRDCDL QRDCDH	Serial data
	QRCTSL QRCTSH	Clear to send
	QRCXL QRCXH	Serial clock
	QRDIL QRDIH	Data

When power is turned on in the tape transport drive before communications occur between the DCC and the tape unit, a power-up reset circuit resets the CPU, the SSDA, and the drive status data register. Upon power up, the D-tape I/O channel is initialized by the DDPU. Drive status words are sent to the DDPU as tape drive control signals to and from the tape transport as shown in Table 3-265.

Upon channel initialization, the tape interface awaits transmission by the DDPU of a tape command code. Whenever awaiting a command, the interface reflects back to the DDPU any byte received on the I/O channel, interprets the byte as a command from the DDPU, and takes the appropriate action. A list of the command codes utilized is given in table 3-266.

Five input signals (defined in drive status word no. 2 table 3-265) to the tape transport interface from the tape transport drive (CIP, FUP, BLB−, ULS−, LLS−) are gated through tri-state line receivers before being fed to the CPU data bus. A dip switch (S1) mounted on the CCA is used as a track write protect safety switch for tracks 1, 2, and 3. These three signals (TR1, TR2, and TR3) are also gated through tri-state line receivers to the data bus. Track 4 is not protected (no connection).

Table 3-265 (U) Tape Drive Status Signals (U)

Bit	Drive Status Word No. 1		Drive Status Word No. 2	
0 (LS)	REV−	Reverse	CIP	Cartridge in Place
1	HSP−	High speed	FUP	File unprotected
2	FWD−	Forward	BLB−	Light bulb on
3	HIT−	High threshold	ULS−	Upper light sensor
4	WEN−	Write enable	LLS−	Lower light sensor
5	ERA−	Erase	Track No. 1	Protect
6	TR-1	Track Select 1	Track No. 2	Protect
7 (MS)	TR-2	Track Select 2	Track No. 3	Protect

A one-shot oscillator controls the proper tape motion in the tape drive. Input RDA− (read data) to the interface CCA from the tape drive, together with FWD−, triggers one-shot oscillator circuits SN74123s and clock timing circuits for the SSDA control signals, RXC (receive clock), RXD (receive data), and DCD− (data carrier detect). The R6 trim pot adjusts the oscillator pulse width for proper operation of the tape drive motor servo circuit. Use test point J-5 for a waveform as shown in figure 3-119.

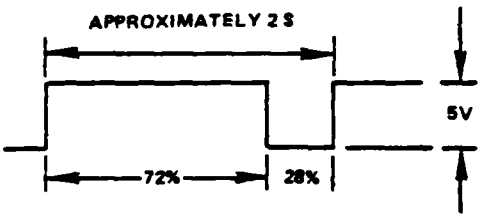


Figure 3-119 (U). Test Point J-5 Waveform (U)

c (U). Low voltage power supply − 5A1PS1.(U) The internal power supply located at the rear of the transport assembly provides +5 VDC, +28VDC and -28 VDC to the tape transport drive and +5 VDC to the tape interface CCA. This power supply

NOTE

There may not be identifying component markings on the tape transport interface CCA; refer to figure 3-120 (U) for location of J-5.

Table 3-266 (U). Tape Controller Command Codes (U)

COMMAND CODE (OCTAL)	FUNCTION
000	Stop the drive
001	Select track 1
002	Select track 2
003	Select track 3
004	Select track 4
005	Drive status request
006	Test pattern request
007	Test echo request
010	Rewind to BOT
011	Space backwards one block
012	Read block
013	Write block
014	Space forward one block
015	Erase
All others	Command echo with illegal command status

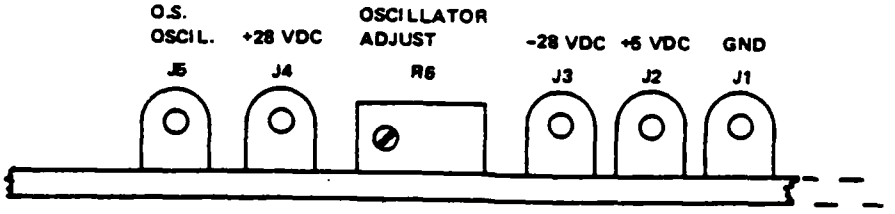


Figure 3-120 (U). Test Points on Tape Transport Interface – 5A1A1 (U)

can be accessed only through the rear of the 5A1 transport assembly. DC power remains on standby status when the display console is on standby, and is readied when the PRGM LOAD pushbutton is pressed for display initialization. This supply receives its input, 115 VAC, 400 Hz, from the ship power system.

d (U). Fan – 5A1B1.(U) Cooling air for the transport assembly is provided by the blower, which operates from 115 VAC, single-phase, 60 Hz power, and is accessed from the rear panel of the unit. Application of power to the blower is controlled by the thermal switch.

3-281(U). OPERATOR DISPLAY AND CONTROL CONSOLE.(ODCC).(U) The overall organization of the ODCC main assemblies is shown in figure 3-121. In Volume V, figure 5-52, the same organization is shown but with detailed interconnections between major assemblies. Numerous operational and test functions are performed by these DCC assemblies. They are described in detail as functional descriptions in various paragraphs that follow. Descriptions of the DCC controls and indicators are presented in chapter 2. A thorough knowledge of the operational effect of the use of these controls and indicators is necessary for a full comprehension of the DDC functional descriptions.

a(U). Overhead assembly – 5A2A1.(U) The overhead assembly comprises the following units.

(1)(U). CONSOLE BREAKER – CB1.(U) This is a two-position on/off switch/circuit breaker providing 3-phase, 400 Hz power to the DCC.

(2)(U). SYSTEM POWER switch – S2.(U) This five-position, rotary switch controls system primary power, antenna servo power, ESM power, and AECM power.

(3)(U). ILLUMINATION controls – R1, R2A, and R2B.(U) These control illumination to two upper floodlights on overhead panel and brightness of all DCC control panel indicators.

(4)(U). LAMP TEST control – S1.(U) This is a pushbutton initiating a lamp illumination test of all console indicator lamps, except the CHAFF LAUNCHER power indicators.

(5)(U). Miscellaneous.(U) These are an upper and a lower flood light (D57 and D58) and a speaker(LS1) for alarm alert audio.

(6)(U). Overhead module – A2.(U) The overhead module is a circuit card assembly that translates switch data from the overhead panel and interlocks to serial data for controls interface module 5A2A5A9.

(7)(U). BATTLESHORT switch – S3.(U) This is a two-position toggle switch that controls power to the battleshort relays.

(8)(U). PROGRAM LOAD control – S4.(U) This pushbutton is used to reset the DCC and initiates program loading from the CTT.

(9)(U). Cartridge tape transport (CTT) – 5A1.(U) The CTT is a magnetic tape transport drive with associated circuits providing a means for loading digital data from a tape cartridge to the DDPU and DPU.

b(U). Filter – 5A2FL1.(U) This filter is in line with the 115 VAC, 400-Hz, 3-phase input power before it is applied via the overhead panel to various power supplies in the DCC.

c(U). OVERTEMP switch – 5A2S1.(U) This switch generates an over-temperature signal when activated. This signal is sent via the overhead panel assembly to the controls interface module in the logic unit. Here, it is converted to a serial data sent to the auxilary panel assembly.

SPEAKER CONTROL input signal goes LOW, the speaker is turned on. When input signals MAJOR ALERT and AUDIO/VIDEO are low, a 1 kHz signal is generated on the SPEAKER and LEFT HEADSET output lines. The outputs of the 1 kHz oscillators are applied to the inputs of the related AND gate, the output of which is fed to a mixer amplifier. The output of the mixer amplifier is applied to the output signals LEFT HEADSET and AUDIO GAIN. The audio gain controls the LEFT HEADSET level. The output of the mixer amplifier is also applied to the input of another amplifier, the output of which goes to the SPEAKER GAIN and to the input of the driver. The driver is a power amplifier that drives the speaker on output line SPEAKER OUTPUT.

When input signals MINOR ALERT and AUDIO/VIDEO SELECT are LOW, a 500 Hz signal is generated on the SPEAKER and LEFT HEADSET output lines. The output of the 1 kHz oscillator is divided by two and applied along with the other 500 Hz oscillator output to the inputs of the related AND gate. The result is a 500 Hz signal that is fed to the audio outputs of the module.

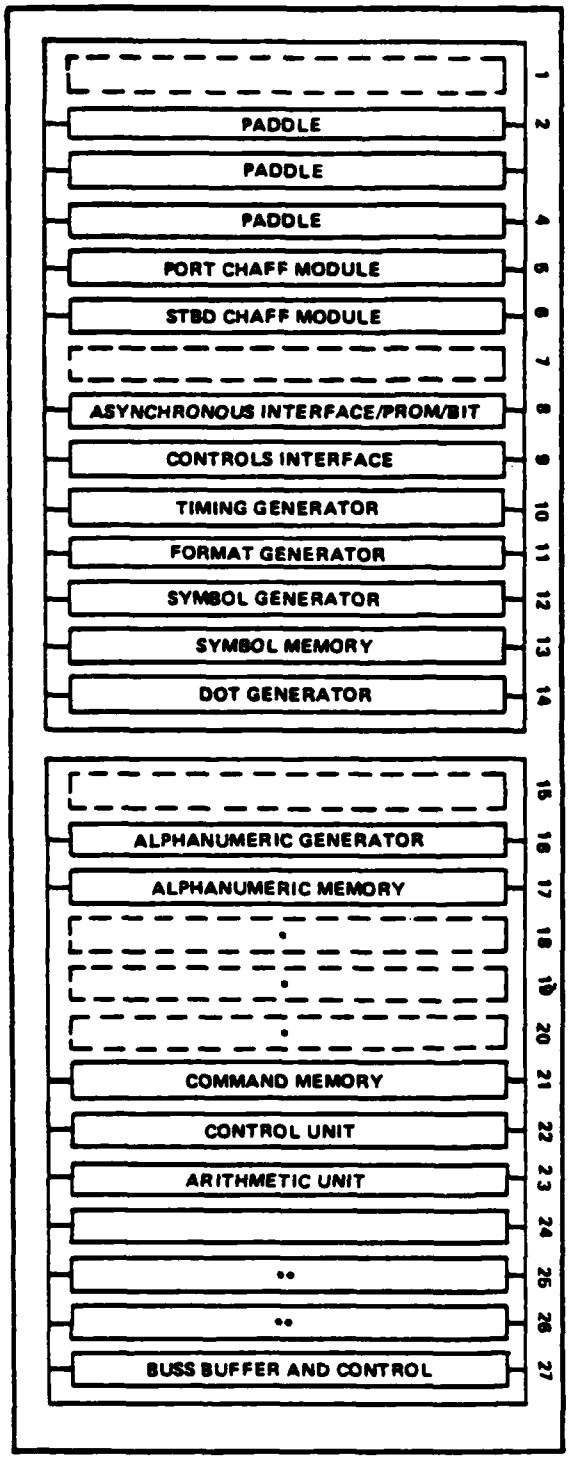
The video tone circuit consists of an input buffer amplifier and a driver pulse stretcher network that contains a low pass filter, and output buffer amplifier and a switch in the form of a logic gate. The input VIDEO signal is amplified by the buffer amplifier, filtered by the driver pulse stretcher network, and amplified by the output buffer amplifier. The resultant audio output represents the video tone that is applied to the input of the switch. When the AUDIO/VIDEO SELECT input is HIGH, the video switch is enabled and the video tone signal is routed to the SPEAKER, GAIN, and HEADSET output lines via the mixer and driver amplifiers. During the time that the video tone circuit is activated, the MINOR and MAJOR ALERT circuits are automatically inhibited.

c(U). Foot switch control circuit.(U) The operator's microphone is disconnected until he engages the foot switch control. The foot switch control circuit (sheet 1) consists of a preamplifier, a microphone gain potentiometer, a FET, and an output driver. During normal operation, the foot switch contacts are open; this causes the field effect transistor switch to remain open. As a result, voice communication between the operator and other shipboard stations flows from the microphone through the preamplifier and the summing amplifier. The output of the summing amplifier drives the RIGHT HEADSET and VOICE GAIN output lines. Pressing the foot switch causes the field effect transistor switch to close, thus activating the output signals 1 thru 5 and SYSTEM via the FET switch QI driver outputs A thru F. The RIGHT HEADSET and VOICE GAIN outputs are also activated.

3-288(U). LOGIC UNIT — 5A2A5.(U) Fifteen digital circuit cards and three paddle cards (connectors) comprise this unit. The interconnections of these cards are shown in Volume V, figure 5-525. Figure 3-131 shows the various cards and their locations in the logic unit card basket. Note that locations (slots) not used are indicated with broken-line enclosures. An asterisk (*) indicates where a slot is not currently used but where the backplane pins are wired for possible use. Two card slots (25 and 26), designated with two asterisks, are wired at the backplane. These slots are reserved for use by circuit cards required during manufacturing test.

The functional interrelations of the circuit cards in the logic unit are shown in figure 3-132. The main interface for addresses and data takes place via the bidirectional bus under control of the control unit A22. The control and the arithmetic unit (A22 and A23) comprise the DDPU. Other units in the DDPU group support the DDPU operation. These consist of the asynchronous interface/PROM/BITE A8, the command memory A21 and the bus buffer and control A27. Various types of video generators, associated memories and the timing generator A10 comprise the display group. In addition to the timing generator, these consist of the symbol generator A12 and memory A13, format generator A11, dot generator A14 and the alphanumeric generator A16 and memory A17. In the timing generator, the digital video from these generators are mixed and converted to analog video supplied to display monitor 5A2A2. A part of the operator interface group consists of the controls interface A9, the port chaff launcher A5 and the starboard chaff launcher A6. Other parts of the operator interface group are contained within the shelf 5A2A4, the auxiliary panel 5A2A3 and overhead 5A2A1 panel assemblies. A detailed description of the circuit cards in the logic unit follows.

3-289(U). CHAFF INTERFACE CIRCUIT CARD MODULE (PORT) — 5A2A5A5.(U) The chaff interface circuit card (Volume V, figure 5-52505) generates firing signals that trigger the port chaff launchers and generate operator switch and chaff tube status information. The chaff interface circuit card also sends control signals to the operator shelf, the overhead panel and the auxiliary panel. The clock and data driver circuit, the chaff fire relay circuit and the chaff status output circuit are the major circuits within the chaff interface circuit card.



NOTE: PREFIX NUMBERS AT RIGHTHAND SIDE OF CIRCUIT CARDS WITH 5A2A5 TO DETERMINE REFERENCE DESIGNATION. FOR EXAMPLE, PORT CHAFF MODULE REFERENCE DESIGNATION IS 5A2A5A5.

*BACKPLANE WIRED – CIRCUIT CARD NOT PROVIDED.
**BACKPLANE WIRED – CIRCUIT CARD NOT PROVIDED – USED FOR MANUFACTURING TEST.

Figure 3-131 (U). Layout of Logic Unit Card Basket (U)

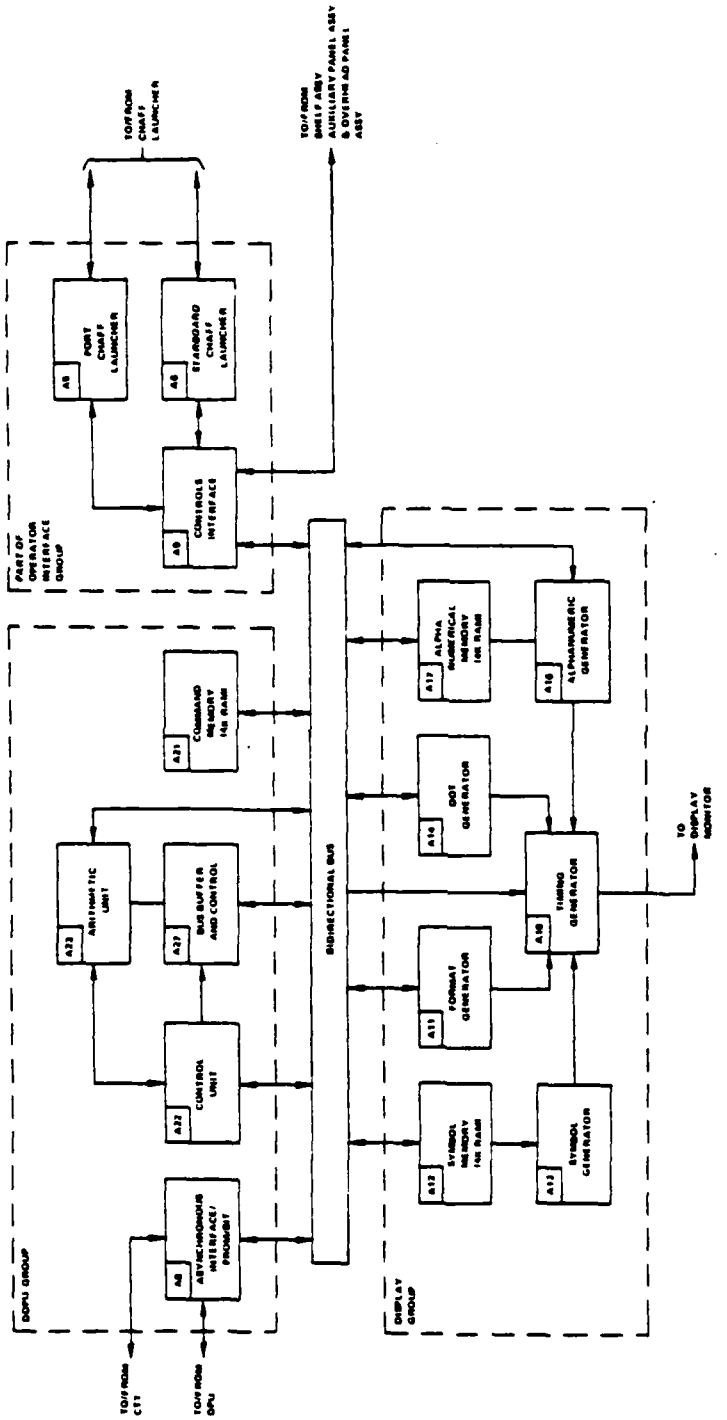


Figure 3-132 (U). Functional Interrelations of Circuit Cards in Logic Unit (5A2A6) (U)

5A2A5A5. The starboard chaff interface circuit card contains two major circuits: the chaff fire relay circuit and the chaff status circuit.

a(U). Chaff fire relay circuit.(U) The chaff fire relay circuit provides firing data to the ship chaff launchers. It consists of one data and address holding register, one chaff status address decoder, one firing relay address decoder, one fire relay data holding register, and fire relays.

The data and address holding register operates as a serial-in parallel-out register. It stores 10 data bits and 2 address bits. The data and address bits are clocked serially into the registers via input lines CTLODCKB1 (clock) and CTLODODB (data and address). Eight of the parallel output data bit lines are applied to the inputs of the fire relay data holding registers. Two data bit lines are applied to the firing relay address decoder. The two address bit lines, with the serial input data line, are applied simultaneously to the firing relay address decoder and the chaff status address decoder. One strobe line is used to select which of the two decoder circuits is enabled. When strobe line CTLODS3D1 goes LOW, it enables the firing relay address decoder. When the strobe line goes HIGH, it enables the chaff status decoder.

The chaff status address decoder applies its five bit output lines to the chaff status shift register inputs SR LOAD ENABLE. These five input lines determine which of the 30 status bits from the optical isolators and signal SPEDINTERLCK are to be loaded into the chaff status shift registers. The status bits are loaded into the chaff status shift registers when the strobe signal CTLODS3D1 goes high. The firing relay address decoder applies its two output lines to the clock inputs of the fire relay data holding registers. These clock inputs load the parallel data bits from the data and address holding registers into the fire relay data holding registers. The data stored in the fire relay holding registers with the two decoder clock pulse determine which launches are fired. This is accomplished by receiving chaff launcher firing information via controls interface module 5A2A5A9 on serial data line CTLODODB. The outputs to the fire relays are LOW when activated. The signal MSTCL-A resets the fire relay data holding registers. Consequently, all the fire relay outputs are disabled. The relay output line consists of six starboard forward lines with four common return lines and six starboard aft lines with four common return lines.

b(U). Chaff Status circuit.(U) The chaff status circuit provides the operator with information about which chaff launchers are full or empty. The chaff status circuit consists of 30 optical isolators, one chaff status shift register and one five-input NOR gate. The optical isolators are used to provide isolation between the 28V chaff launcher signals and the 5 V logic of the chaff modules. The optical isolators couple the status of the chaff launchers to the chaff status shift registers. The five outputs of the chaff status register are applied to the five inputs of the NOR gate. The NOR gate serial output is inverted and outputted as serial data on line TUBE DATA OUT. This serial data contains the status information of the chaff launchers (loaded or empty). The status information is supplied to the controls interface module where it is processed and returned to the chaff interface module via input data line CTLODODB.

Parallel data loading of the chaff status shift registers occurs on the rising edge of the clock pulse while the SR LOAD ENABLE signals are LOW. The parallel data is shifted out serially and is coincident with each successive clock pulse. During this time, the SR LOAD ENABLE signals are held high. Therefore, the 30 inputs from the port starboard chaff launchers and the input SPEDINTERLCK are parallel-loaded into the chaff status shift register and converted to serial outputs on output line TUBE DATA OUT.

3-291(U). ASYNCHRONOUS INTERFACE/ PROM/BIT — 5A2A5A8.(U) The asynchronous interface/PROM/BIT (Volume V, figure 5-52508) consists of: an asynchronous communications interface adapter (ACIA) for direct data transfer between the DPU and DDPU and the cartridge tape transport (CTT) 5A1 and DDPU; a bootstrap loader for loading DPU programs from the CTT 5A1 under control of the bootstrap PROM; and BIT indicators for displaying results of BITs that are run with the loading of programs by the bootstrap loader.

An overview of the asynchronous interface/ PROM/BIT functions is shown in figure 3-133. The two types of data transfers, serial and parallel, take place as follows:

Serial data transfers between either the DPU or the CTT and the ACIAs

Bidirectional parallel data transfers between the ACIAs and the DDPU

By combining these two types of transfers, communication between the following various functional units is accomplished.

CTT to DPU
DPU to CTT
DPU to DDPU
DDPU to DPU

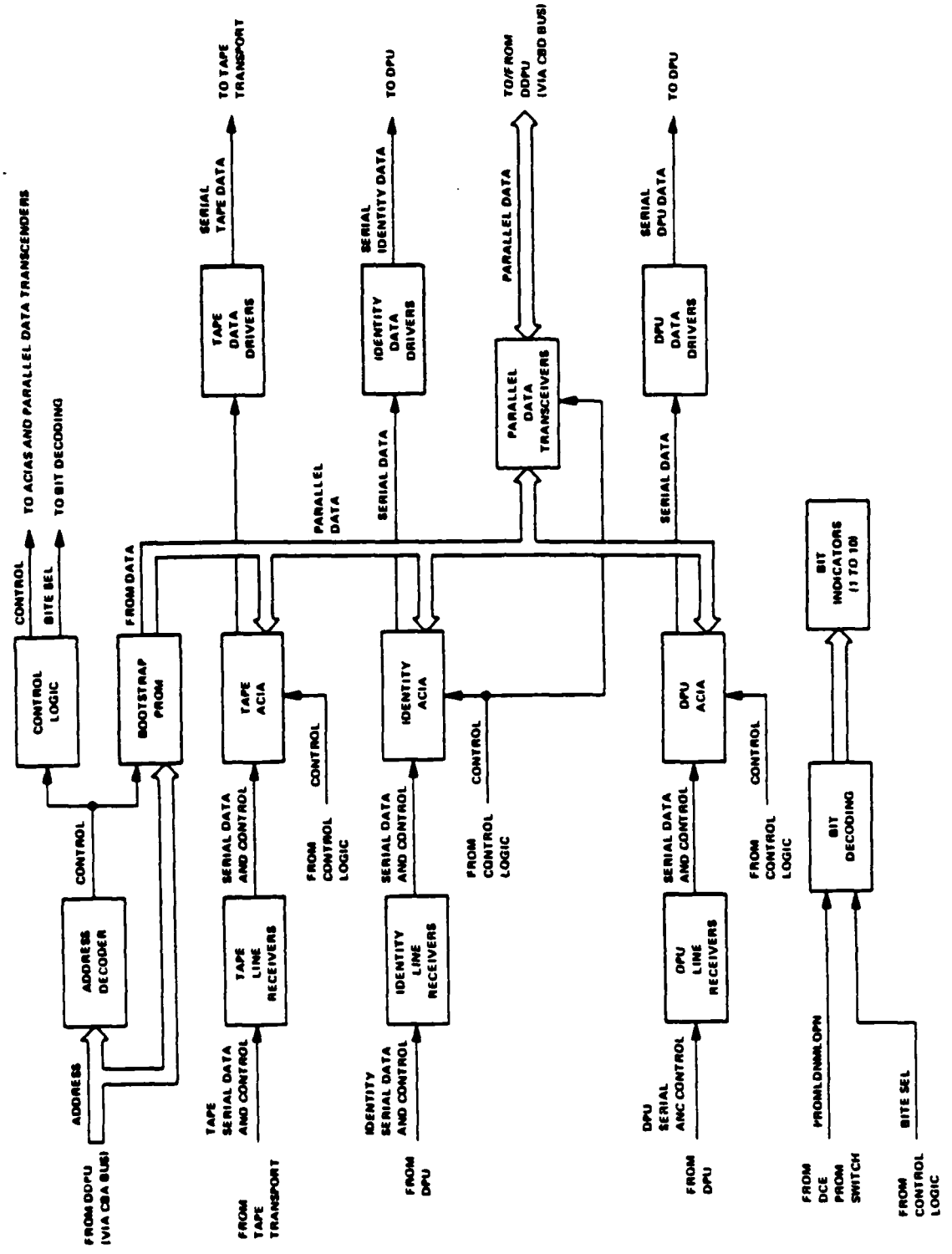


Figure 3-133 (U). Overview of Asynchronous Interface/PROM/BIT (U)

To accomplish communication between the CTT and the DPU, serial data is routed by the tape line receivers through the tape ACIA to the DDPU by way of the parallel data transceivers as tape parallel data. The tape parallel data is routed next by the parallel data lines and the parallel data transceivers to the identity and the DPU ACIAs and, then by the serial data lines and data drivers, to the DPU. These communications are controlled by the DDPU, the DPU and the CIT being slaved to the DDPU. Below is a graphic representation of the communication flow described and the three other types of flow.

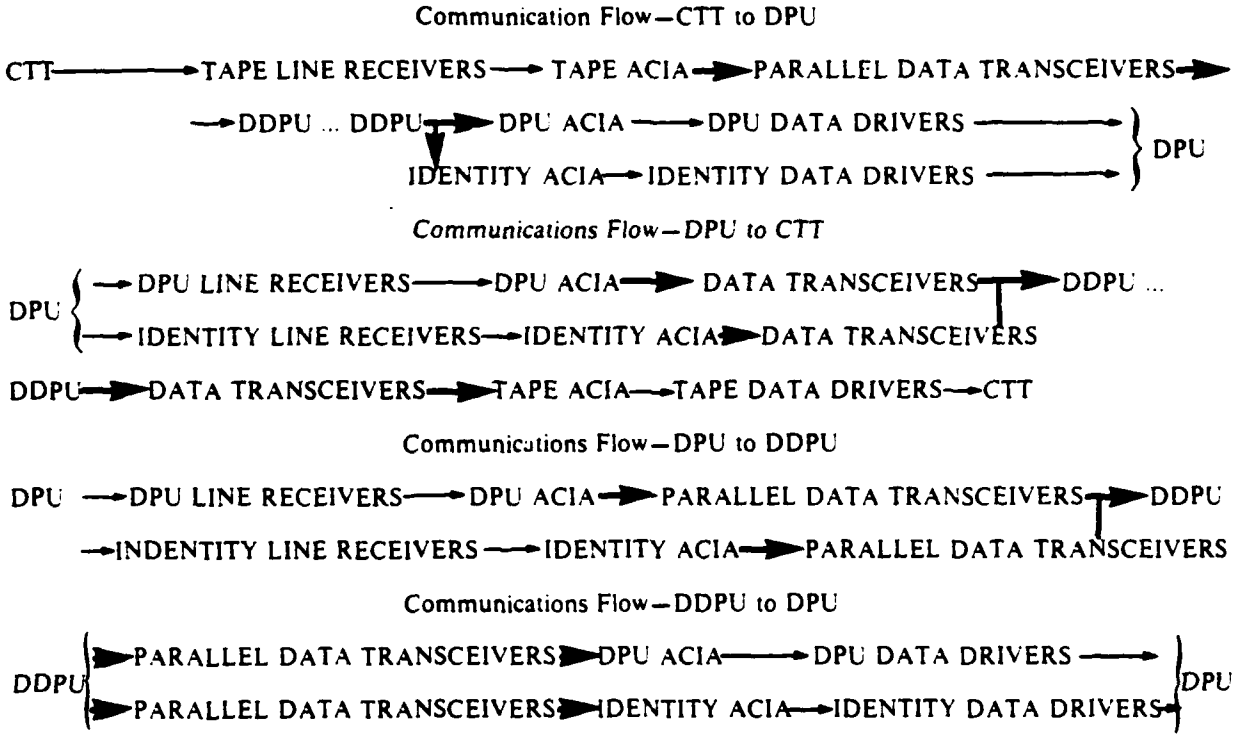


Figure 3-134 (U). Communications Flow (U)

The parallel output lines of the transceivers are tied to the CBD-bus. The CBA-bus is tied to the address decoder and the bootstrap PROM. Addresses from the DDPU are inputted to the address decoder, which produces control signals that are used by the control logic. One of these control signals connects to the bootstrap PROM and enables the reading of data from the bootstrap PROM to the DDPU by way of the parallel data transceivers and the CBD-bus. Control signals produced by the control logic are used for enabling the data transceivers for reading and writing, for conditioning the bit decoding logic, and for relating the ACIAs for read/write operations.

a(U). ACIA.(U) The following is a description of the typical operation of an ACIA. Refer to figure 3-135 for a simplified block diagram of the main functional units comprising an ACIA.

During power-on reset/master clear reset, a power-on reset circuit within the ACIA detects the power line turn-on transition and holds the ACIA in a reset state until initialization is complete. This prevents erroneous output transitions. Before data transmission can occur, the ACIA must be initialized by a programmed initialization routine. This routine master resets the ACIA and performs certain other initialization programming of the ACIA control register. After completion of initialization, the ACIA may be used for transmitting and receiving data.

Each ACIA converts 8-bit DDPU parallel data byte information into a serial data format for transmittal to either the DPU or the CTT, and vice versa. The serial data format consists of a serial bit stream that comprises a start bit, eight data bits, and a stop bit. The start and stop bits are added to each serial data byte derived from the parallel data byte. The converse is

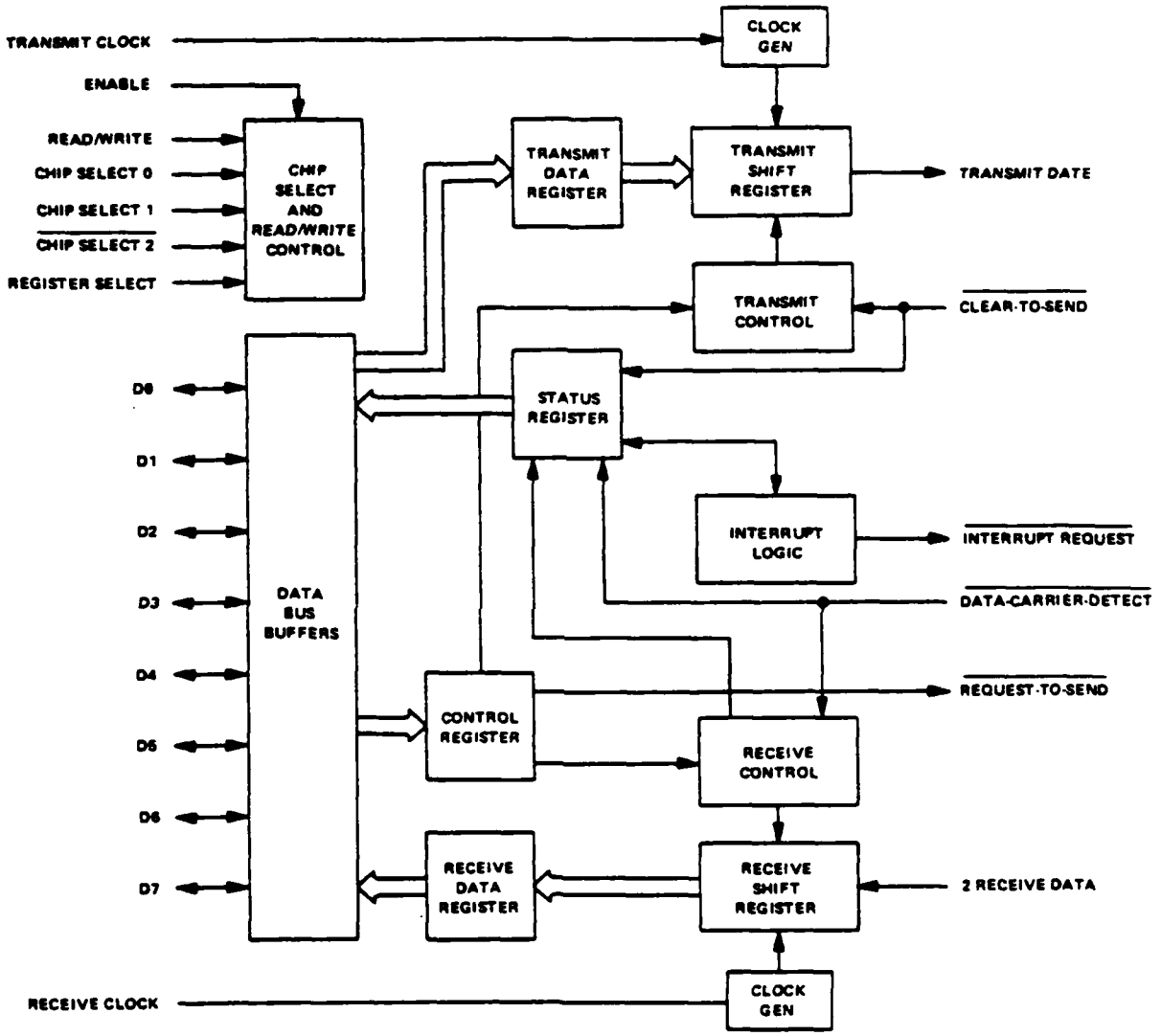


Figure 3-135 (U). Typical ACIA, Simplified Functional Block Diagram (U)

true for the conversion of serial to parallel data The start and stop bits are deleted by the ACIA. The ACIA is also capable of adding a parity bit to form the serial data byte or deleting the parity bit to form a parallel data byte. However, this parity-bit addition or subtraction is not accomplished in the described use of the ACIA. Thus, the parity generator function is not shown in figure 3-135

Except for input/output signals to the ACIA device, the block diagram of figure 3-135 does not show signal names on the lines that interconnect the various ACIA functional units. These internal lines show only the actual interrelation of the functional units and the direction of signal flow.

(1)(U). Transmitting serial data.(U) A serial data transmitting sequence starts with the parallel data byte already in the data bus buffers. As a result of an interrupt, the status register is queried and, if the transmit data register is empty, the parallel data byte in the bus buffers is read into the shift register. There, the data byte is serialized. One start bit and one stop bit are added to the data stream, and the byte is transmitted out of the ACIA via the transmit data line to the receiving peripheral device. After the first byte is read into the transmit data register, the status register is queried again to determine if the transmit data register is empty and the peripheral device status is checked. If the register is empty, another byte can be read into the transmit data register even if the preceding byte is still being transmitted from the transmit shift register. The second byte is transmitted into the transmit shift register as soon as the first byte has been shifted out. This sequence of operation continues until all bytes have been processed.

(2)(U). Receiving serial data.(U) A serial data byte, received from the peripheral by way of the receive data line, is shifted into the receive shift register. The status register is queried to determine if the receive data register is full. If the register is full, the serial data byte is placed on the 8-bit ACIA bus when a read data command is received from the DDPU. Both the start and stop bits are stripped from the byte and only the data bits are transferred via the data bus buffers to the DDPU. The contents of the next byte are automatically shifted from the receive shift register to the receive data register. The status register is repeatedly queried to determine if the receive data register is full. This sequence of operation is continued until all serial data bytes have been received, converted to parallel data bytes, and outputted by way of the bus buffers and DDPU data bus. Note that throughout the sequence, data bytes may be read from the receive data registers while the next byte is being written into the receive shift register.

(3)(U). Input/output functions.(U) Each ACIA interfaces to the DDPU via a bidirectional data bus. Only 8 bits of data comprise the parallel data byte of one ACIA. Some data transfers require only one 8-bit byte, whereas some transfers require one 8-bit byte plus two 8-bit bytes, the latter requiring one 16-bit word. The DDPU data bus can handle 16 bits and, thus, can accommodate both types of transfer. When not required, the 8 MSBs of the data bus are not used.

Various control signals are used in the ACIA-DDPU interface; there are three chip-select signals, a register select signal, an interrupt request signal, a read/write control signal and an enable signal. These signals, with various DDPU programming subroutines, control the operation of the ACIA. Following are descriptions of these control signals and their effects upon the operation of the ACIA.

(a)(U). ACIA bidirectional data (D0 thru D7).(U) Data bits 0 through D7 are the parallel data bits that are loaded onto the DDPU CBD bus. The ACIA data drivers are tri-state devices that are held in the high-impedance state except when the DDPU reads data from the ACIA.

(b)(U). ACIA enable.(U) The enable signal is a high-impedance, TTL-compatible input to the ACIA that enables the ACIA input/output data bus buffers and thus clocks data into or out of the ACIA.

(c)(U). Read/write.(U) The read/write signal comes into the ACIA over a high-impedance, TTL-compatible line. The state of this signal controls the direction of data flow through the input/output data bus interface. When the read/write signal is HIGH, the ACIA output buffers are enabled and a data byte is read from a selected register to the DDPU. When this signal is LOW, the ACIA output drivers are disabled, and the DDPU writes a data byte into a selected register. Later in this discussion, the various registers that take part in read and write transmissions are described.

(d)(U). Chip select (CS0, CS1, and CS2).(U) These three signals are transmitted to the ACIA over high-impedance, TTL-compatible lines. These signals select the ACIA when CS0 and CS1 are HIGH and CS2 is LOW. Once the ACIA is selected, data byte transfers are controlled by the enable, read/write, and register select signals.

(e)(U). Register select (RS).(U) This signal is transmitted to the ACIA over a high-impedance, TTL-compatible line. A high-level signal selects either the transmit or the receive data register, whereas a low-level signal selects either the control or

the status register. The state of the read/write signal determines the particular read-only or write-only register (of the particular register pair) that is to be selected.

(f)(U). Interrupt request.(U) The interrupt request signal is transmitted from the ACIA via a TTL-compatible, open-drain (no internal pullup) line. This signal is an ACIA active-LOW output that interrupts the DDPU. The interrupt request remains LOW as long as the cause of the interrupt is in effect and the appropriate interrupt enable within the ACIA is in the active state.

Interrupts occur for transmit operations, receive operations, and detection of a loss of carrier. Data carrier detect goes LOW. Transmit interrupts occur when the transmit interrupt within the ACIA is enabled and the transmit data register is enabled; this interrupt is cleared by writing data into the transmit data register. Receive interrupts occur when the receive interrupt within the ACIA is enabled and the receive data register is full, when an overrun is detected (indicating a data receive discrepancy), and when a loss of the data carrier is detected.

(g)(U). Clock inputs.(U) Separate high-impedance, TTL-compatible inputs to the ACIA are provided for clocking transmit and receive data. Transmit data is initiated on the negative transition of the transmit clock; this clock synchronizes the transmit data stream. The receive clock synchronizes the receive data stream using the positive transition of the clock.

(h)(U). Serial input/output.(U) There are two types of serial transfers, transmit data and receive data. Serial data is transferred to a peripheral, either the DPU or the CTT, from the transmit shift register via the transmit data line. Serial data is received by the receive shift register via the receive data line.

(i)(U). Peripheral control.(U) Following are descriptions of several signals that exercise some control of serial data transmissions:

Clear-to-send – This high-impedance, TTL-compatible input to the ACIA transmit control and status registers, when LOW, enables reading of data to the transmit shift register. A high-level input inhibits data transmission.

Request-to-send – The request-to-send signal is an active low signal that is output from the ACIA when it is ready to transmit data. This signal is turned around and sent back to the ACIA as clear-to-send (active LOW).

Data Carrier Detect – This signal is sent from a peripheral to the ACIA receive control and status registers over a high-impedance, TTL-compatible line. In its active LOW state, it indicates to the ACIA that the peripheral is ready to commence a serial data transfer. A LOW-to-HIGH transition indicates a loss-of-carrier condition, resulting in both the ACIA interrupt logic putting out an interrupt request signal and the cessation of further transmission of data. (In the DCC ACIAs, the tape ACIA uses this signal, whereas the identity and DPU ACIAs do not use it. In the latter cases, the data-carrier-detect signal is tied to ground, thus remaining constantly in the active-LOW state.)

(4)(U). ACIA registers.(U) The block diagram of figure 3-135 shows the registers and other units that are internal to the ACIA. These registers are of two types, data processing and control. The data processing registers are those through which serial or parallel data bytes pass, whereas the control registers receive or transmit control signals to or from units outside of the ACIA. These registers also produce control signals (not identified in figure 3-135) that are used within the ACIA. Descriptions of the four registers that exercise the main data processing and control are described below. Table 3-268 summarizes the contents of the transmit data register, status register, control register, and the receive data register.

(a)(U). Transmit data register.(U) Data is written into this register during the negative transition of the enable signal when the ACIA has been addressed and RS · R/N (register select and read/write) are selected. Writing data into this register causes the transmit data register empty bit (TDRS) to go LO, thus enabling the transmission of data. If the transmitter is idling and no data is being transmitted, the transfer starts within one bit time of the trailing edge of the write command. If a data byte is being transmitted, transmission of the next data byte starts as soon as transmission of the current data byte ceases. Transfer of data from this register causes TDRE to go HIGH, thus indicating that the register is empty.

(b)(U). Receiver data register.(U) Data is automatically transferred to an empty receive data register from the receive shift register in parallel form when the shift register has received a complete data byte. Loading of the receive data register causes the read data register full bit (RDRF) in the status register to go HIGH, thus indicating a register-full

Table 3-268 (U). Contents of ACIA Registers (U)

Data bus line no.	RS · R/W transmit data register (write only)	RS · R/W receive data register (read only)	RS · R/W control register (write only)	RS · R/W status register (read only)
0	Data bit 0	Data bit 0	Counter divide select 1 (CR0)	Receive date register full (RDRF)
1	Data bit 1	Data bit 1	Counter divide select 2 (CR1)	Transmit data register empty (TDRE)
2	Data bit 2	Data bit 2	Word select 1 (CR2)	Data-carrier-detect (DCD)
3	Data bit 3	Data bit 3	Word select 2 (CR3)	Clear-to-send (CTS)
4	Data bit 4	Data bit 4	Word select 3 (CR4)	Framing error (FE)
5	Data bit 5	Data bit 5	Transmit control 1 (CR5)	Receiver overrun (OVRN)
6	Data bit 6	Data bit 6	Transmit control 2 (CR6)	Parity error (PE)
7	Data bit 7	Data bit 7	Receive interrupt enable (CR7)	Interrupt request (IRQ)

status. Data then may be read out of the receive data register by the data bus buffers addressing the ACIA and selecting the receive data register (RS and R/W both HIGH) when the ACIA is enabled. This is a nondestructive read, but it causes the RDRF bit to be cleared to indicate a register-empty status (although data is retained in the read data register). This empty status is maintained by the receive data register full (RDRF). The fact that the read data register is full inhibits the automatic transfer of data from the receive shift register. The contents of the read data register remain valid with the current status stored in the status register.

(c)(U). Control register.(U) There is a separate control register in the ACIA. Thus, control codes and read status communications may occur at any time under control of a DDPU service routine. This feature eliminates the chance of scrambling data that is ready to be transmitted. There are eight bits in the control register; the functions of these bits are identified in table 3-268. Only those bit functions applicable to the ACIA as used in the DCC are described; other functions are shown only for completeness.

1(U). Counter divide select bits (CR0 and CR1).(U) These bits determine the divide-ratio utilized both in the transmitter and the receiver sections of the ACIA. For the DCC application, these bits are both 0, providing a divide-by-1 ratio. Additionally, these bits provide a master reset for the ACIA, thus clearing the status register and initializing the receiver and transmitter sections of the ACIA. After a power-on or a power-fail/restart, these bits are set HIGH to reset the ACIA. After resetting, the clock divide ratio is selected.

2(U). Word select bits (CR2, CR3, and CR4).(U) The word select bits select the word length and the number of stop bits (only one for the DCC). The state of these bits for the ACIA are logic 1 (HIGH) for CR2, logic 0 (LOW) for CR3, and logic 1 (HIGH) for CR4.

Table 3-269 (U). Transmitter Control Bit Truth Table (U)

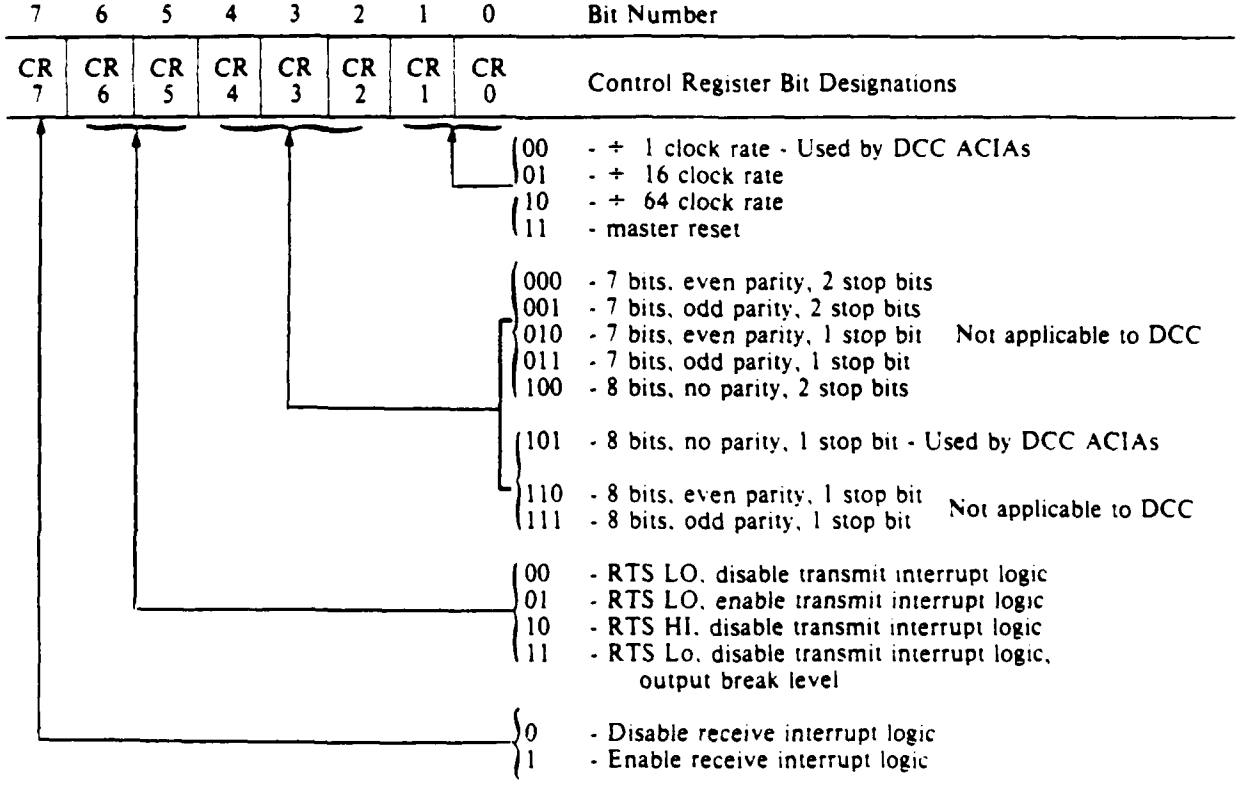
CR6	CR5	Function
0	0	$\overline{RTS}$ LO; transmitting interrupt disabled.
0	1	$\overline{RTS}$ LO; transmitting interrupt enabled.
1	0	$\overline{RTS}$ HI; transmitting interrupt disabled.
1	1	$\overline{RTS}$ HI; transmit a break level (space) on the transmit data output line; transmitting interrupt disabled.

3(U). Transmitter control bits (CR5 and CR6).(U) Two transmitter control bits control the interrupt from the transmitter data register empty condition and the request-to-send (RTS) output. Table 3-269 is the truth table for CR5 and CR6.

4(U). Receive interrupt enable bit (CR7).(U) The following interrupts are enabled by a high level of CR7: receive data register full, overrun (resulting from receive serial data being transferred from the receive shift register to the receive data register before current contents of the latter are transferred, and a LOW to HIGH transition of the $\overline{\text{data-carrier-detect signal}}$.

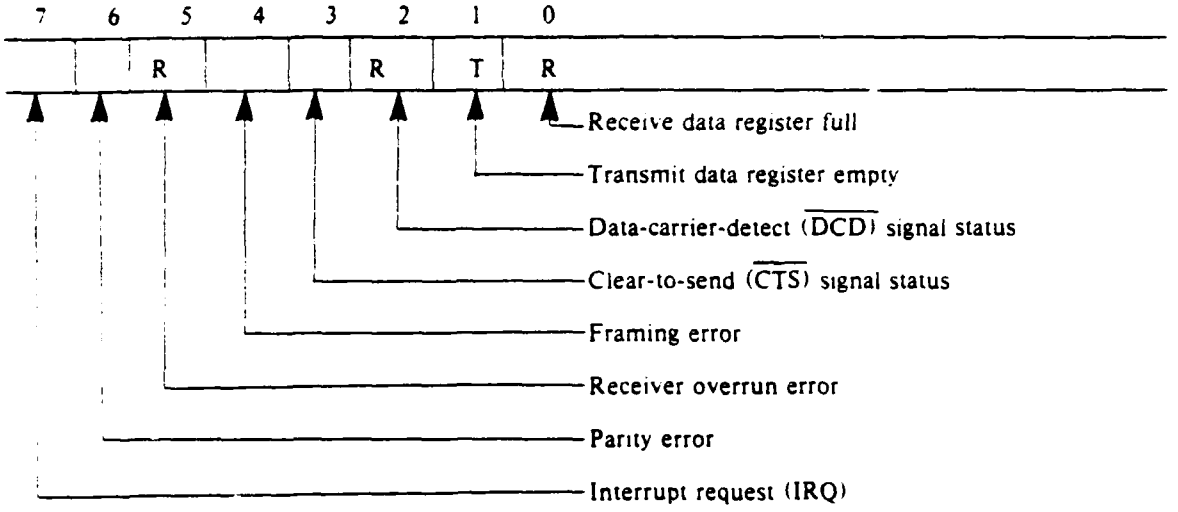
The interpretation of the functions of the control register is summarized in table 3-270.

Table 3-270 (U). Control Register Functions (U)



(d)(U). Status register (U) There are four types of information that are contained in the 8-bit status register: transmit status, receive status, error indications, and interrupt request. This information may be read by the DDPU (when register select is LOW and read/write is HIGH). The status indications for the various bits are listed in table 3-169 and are summarized below.

Table 3-271 (U) ACIA Status Summary (U)



T—indicates that an interrupt request occurs from transmit logic
R—indicates that an interrupt request occurs from receive logic
Note than no interrupt request occurs for status bit positions not having a T or an R.

A logic 1 (HIGH) in any of the bit positions identified with either a T or an R causes an interrupt request to occur except for status bit position 3, data-carrier-detect. Here, the transition of data-carrier-detect from a logic 0 (LOW) to a logic 1 (HIGH) causes an interrupt request to occur. In any case, the interrupt logic is enabled. Note that either transmit logic or receive logic may be enabled separately. The control register bits 5 and 6 determine whether or not transmit or receive interrupt logic is enabled. Control register bit " determines whether or not receive interrupt logic is enabled. Note that the condition of status register bit 3 also can disable an interrupt request for the transmit-data-register-empty condition.

Clearing of an interrupt request results from various conditions that depend upon the cause of the interrupt:

An interrupt request for the receive-data-register-full condition is cleared if the DDPU reads data from the ACIA or if a reset control code is issued.

An interrupt request for the transmit-data-register-empty condition is cleared by writing data to the ACIA or by issuing a reset control code

An interrupt requested by a data-carrier-detect (DCD) or an overrun is cleared by reading the status register after the error condition takes place and then reading the data register. A master clear also clears these interrupt requests

Following are descriptions of the way that the various bits of the status register are affected by operation of the ACIA.

1(U). Status register bit 0, receive data register full.(U) This bit goes HIGH to indicate the receive data register is full (has received data from the receive shift register). This bit is cleared (goes LOW) after the data is read by the DDPU and then indicates an empty condition. Data carrier detect in the HIGH state also causes bit 0 to indicate empty (LOW). This latter feature prevents reading of invalid data by the DDPU.

2(U). Status register bit 1, transmit data register empty.(U) When HIGH, this bit indicates that the contents of the transmit data register have been transferred and the next byte of data may be loaded. When LOW, this bit indicates that the transmit data register is full and that loading of the next byte has not begun since the last write command.

3(U). Status bit 2, data-carrier-detect.(U) When HIGH, this bit indicates that the data-carrier-detect signal to the ACIA has gone HIGH to indicate that a carrier is not present. The transition of this bit from a LOW to a HIGH state also causes an interrupt request to be generated when the receive interrupt enable (bit 7 of the control register) is enabled (HIGH). Status bit 2 remains HIGH even after the data-carrier-detect signal goes LOW and then is cleared (goes LOW), first by reading the status register and, second, by reading the receive data register. If a master reset occurs, status bit 2 is cleared. If the data-carrier-detect signal remains HIGH after both a read-status and a read-data operations or after a master reset, the interrupt is cleared and the data-carrier-detect status bit remains HIGH, and then, is conditioned subsequently by the data-carrier-detect input signal.

4(U) . Status bit 3, clear-to-send.(U) This bit indicates the state of the clear-to-send input signal from a peripheral (either the DPU or the CTT). When HIGH, this bit inhibits the effect of the transmit-data-register-empty status bit (bit 1). When LOW, this bit indicates that there is a clear-to-send input to the ACIA from a peripheral. A master clear does not affect the clear-to-send status bit.

5(U). Status bit 4, framing error.(U) This bit, when HIGH, indicates that the received data byte is not properly framed by a start and a stop bit. This condition is detected by the absence of the stop bit. A synchronization error, faulty transmission, or a break condition (all spaces) is thus indicated. This bit is either set or reset during a receive-data transfer and is present, therefore, throughout the time that the associated data byte is current.

6(U). Status bit 5, overrun error.(U) A HIGH state of this bit indicates receiver overrun, a condition resulting from having received a data byte in the receive data register but having loss (not read) one or more bits before the transfer of the next byte to the receive data register. Status bit 0 (receive data register full) also goes HIGH due to an overrun. The overrun condition begins at the midpoint of the second character received in succession without a valid read data operation from the receive data register. The overrun bit is set to HIGH upon receipt of the next data read command. This bit is reset to LOW after successfully reading a data byte from the receive data register. Status bit 0 (receive data register full) is reset (to LOW) after status bit 5 (overrun) is reset. During the overrun condition, byte synchronization is maintained.

7(U). Status bit 6, parity error.(U) Parity is not a factor in the ACIA as used in the DCC. Therefore, in this case, both the parity generator output and the receiver parity check results are inhibited.

8(U). Status bit 7, interrupt request.(U) This bit indicates the state of the interrupt request ($\overline{IRQ}$) output of the ACIA. Whenever there is an unacknowledged interrupt request pending at the ACIA, this bit is HIGH and the interrupt request signal is LOW. This bit is cleared (to LOW) by either a read operation by the receive data register or a write operation from the transmit data register.

(5)(U). Functional signal flow of ACIAs.(U) The various ACIAs and related functional units are shown in Volume V, figure 5-52508, the signal flow diagram of the asynchronous/PROM/BIT circuit card. All of the input/output signals are accounted for on this diagram. The signals are defined in alphanumeric order by signal name on the input/output sheets of figure 5-5208. These signals are also listed in table 3-272 and 3-273 according to the various types of communications in which the ACIAs take part. Timing diagrams are included in figure 5-52508.

All communications and data transfers are controlled by the DDPU. The ACIAs are addressed by the DDPU using CBA00− thru CBA15−. The address is decoded by the address decoder, the outputs of which are used by the control logic. Various control signals are produced by the control logic to select the appropriate ACIA and to control the data transfers. The following control signals from the control logic are inputted to the ACIAs: enable, read/write, two chip select signals, and three clock signals. Other ACIA control signals are inputted to the line receivers and from there to the ACIAs. The serial data is routed similarly through the line receivers to the ACIAs. Note that these serial data and controls that are received from the DPU and the CTT are defined in tables 3-272 and 3-273.

The ACIA always convert serially received data to parallel data, which is always transferred to the DDPU. The parallel data from any ACIA is routed via the

Table 3-272 (U) DPU/Tape Transport Interface Signals (U)

Signal Mnemonic	Pin	Name/Function
Tape Receive Signals		
QRCXL	91	Tape Receive clock (LOW)
QRCXH	35	Tape receive clock (HIGH)
QRD1L	90	Tape receive serial data 1 (LOW)
QRD1H	33	Tape receive serial data 1 (HIGH)
QRCTSL	85	Tape clear to send (LOW)
QRCTSH	86	Tape clear to send (HIGH)
QRDCDL	84	Tape carrier detect (LOW)
QRDCDH	83	Tape carrier detect (HIGH)
Tape Transmit Signals		
RQCXL	88	Status transmit clock (LOW)
RQCXH	89	Status transmit clock (HIGH)
RQD1L	87	Tape transmit serial data (LOW)
RQD1H	31	Tape transmit serial data (HIGH)
RPTHI	48	DDPU high level interrupt
QPWRL	82	Power control (LOW)
QPWRH	81	Power control (HIGH)
RQSTRL	14	Tape reset (LOW)
RQSTRH	69	Tape reset (HIGH)

parallel data transceivers to the DDPU. The direction of flow for a parallel transfer is determined by the read/write signals from the control logic. Conversely, all data from the DDPU is routed through the transceivers to the ACIAs.

Serial data transfers and communications from the ACIAs are routed through the data drivers to either the DPU or the CTT. The data bits and control signals involved are defined in tables 3-272 and 3-273.

(a)(U). Address decoder and control logic.(U) An address is transmitted by the DDPU to the address decoder via the CBA-bus (CBA00 thru CBA15). The address is decoded, and the decoder outputs are used by the control logic to determine the mode of operation. CBWRT− and CBRQS− (write and request) are inputted to the control logic and the address decoder, respectively. At the same time, the CBA00 thru CBA15 address is inputted to the address decoder. CBACK− (acknowledge) is generated upon completion of the transfer of the address to the decoder. This signal is transmitted to the DDPU, indicating a successful loading of the address. The control logic produces the control signals that implement the mode of operation resulting from the decoding of the address. Following are the modes of operation:

Tape I/O interface

DPU I/O interface

Bootstrap PROM operation

BIT select indicator operation

Note that there is a CBACK− generated for each mode of operation.

The 1/16 clock is the basic system clock, and is used for synchronization of various controls produced by the control logic.

(b)(U). Bootstrap PROM.(U) The firmware residing in the bootstrap PROM comprises test and loader routines that are used for startup/reinitialization of the DCC. The DDPU transfers control upon power-on or a restart command being generated by pressing and then releasing PRGM LOAD. The bootstrap PROM is addressed via bus lines CBA00 thru CBA09, and it is selected by PROMSEL from the address decoder. PROM data is transmitted to the DDPU over the PROM data 00 through data 15 bus to the parallel data transceivers. From here, the data is loaded on the CBD bus and inputted to the DDPU.

Table 3-273 (U) DPU Serial Interface Signals (U)

Signal Mnemonic	Pin	Name/function
Identity (status) Receive Signals		
URCXL	21	Status receive clock (LO)
URCXH	78	Status receive clock (HI)
URD2L	77	Status receive serial data (LO)
URD2H	76	Status receive serial data (HI)
Identity (status) Transmit Signals		
RUCTSL	25	Status clear-to-send (LO)
RUCTSH	80	Status clear-to-send (HI)
RUCXL	23	Status transmit clock (LO)
RUCXH	79	Status transmit clock (HI)
RUD2L	75	Status transmit serial data (LO)
RUD2H	19	Status transmit serial data (HI)
DPU Receive Signals		
URD3L	65	MSB receive serial data (LO)
URD3H	66	MSB receive serial data (HI)
URD4L	63	LSB receive serial data (LO)
URD4H	62	LSB receive serial data (HI)
URCTSL	73	Status/MSB/LSB clear-to-send (LO)
URCTSH	74	Status/MSB/LSB clear-to-send (HI)
DPU Transmit Signals		
RUDCDL	70	DPU transmit clear-to-send (LO)
RUDCDH	68	DPU transmit clear-to-send (HI)
RUD3L	67	DPU MSB transmit serial data (LO)
RUD3H	11	DPU MSB transmit serial data (HI)
RUD4L	61	DPU LSB transmit serial data (LO)
RUD4H	5	DPU LSB transmit serial data (HI)
DPU Restart Signals		
PROGRAMLDNO	72	Program load switch input (restart)
PGRMLDNMLOPN	92	Program load switch output (restart)

(c)(U). BIT decoding and BIT indicators.(U) During startup/reinitialization, the BIT indicator DS1 is set to 1 (lit) and all other indicators D52 thru 0510 are reset to 0 (extinguished). BIT indicator DS1 is reset after the successful completion of the first BIT instruction sequence, and DS2 is set at the beginning of the next BIT instruction sequence. Upon successful completion of the current BIT instruction sequence, the corresponding BIT indicator is extinguished. The next BIT indicator of the next higher number is set upon commencement of the next BIT instruction sequence. The process continues throughout the startup/reinitialization process. If any BIT instruction sequence is not successfully performed, the BIT indicator for that sequence remains

set (lit) and the remainder of the routines are aborted. The BIT indicators DS1 thru DS10 are exercised twice during the entire DCC PROM loader/BIT program. Table 3-274 defines the significance of the indicators if they remain lit after the completion of the corresponding BIT instruction sequence.

The BIT decoding logic is reset by RESTART. The state of the output lines to BIT indicators DS1 thru DS10 is set to light DS1 and to extinguish DS2 thru 10. As each BIT instruction sequence is processed, BITE SEL updates the BIT decoding logic, which then changes the state of the BIT indicators accordingly.

3-292(U). CONTROLS INTERFACE - 5A2A5A9.(U) The controls interface circuit card (Volume V, figure 5-52509) controls and processes the flow of data between the DDPU and the operator interface subsystem shown in data flow block diagram figure 3-136. The information processed by the controls interface circuit card includes data from the following peripheral devices: operator pushbutton switch data, lamp data, keyboard data, stiff stick data, ship chaff launcher data, and vertical retrace data of the operator display monitor.

Data is transferred between the DDPU and the controls interface via the DDPU 16-bit data bus. Address decoding and write, request, and acknowledge logic are included on the controls interface to accommodate these transfers. Data is transferred between the controls interface and the peripheral devices via serial data lines. Clock and data strobe signals are sent by the controls interface to the peripheral devices. With proper signal termination and device interface driving hardware, the peripheral devices can be located up to 50 feet away from the control interface circuit card.

a(U). Interrupt control.(U) The interrupt control circuit causes a DDPU interrupt when the following conditions occur: when new serial data is received from the peripheral devices, during a polling cycle if there is a change in the serial data, or during the time of each vertical retrace line of the cathode ray tube monitor display.

Table 3-274 (U). BIT Indicator States (U)

BIT indicator DS No.	Definition of BIT instruction sequence
1	Initial LED status failure
2	DDPU self-test failure
3	DDPU program storage RAM test failure
4	Tape echo request command test failure
5	Tape initialization test failure
6	A/N refresh memory test failure
7	A/N generator enable test failure
8	Keyboard/controls communications test failure
9	DDPU tape loader test failure
10	Symbol generator memory test failure
1	Track history generator memory test failure
2	Polar format generator enable test failure
9	DPU interface communications test failure
10	All DCC BIT test passed

SELECTA and SELECTB enable either the C-address bus or symbol address bus to the input address multiplexer. The SELECTB also enables the input data multiplexer.

ADDRESS STROBE− enables the refresh address mutliplexer and, with SELECTB, selects the input data multiplexer.

COLUMN ADDRESS STROBE− clocks in high order address bits to the RAM.

ROW ADDRESS STROBE− clocks in low order address bits to the RAM.

CHIP SELECT STROBE− enables the RAM access.

READ/WRITE− controls RAM read/write.

b(U). Alphanumeric memory/DDPU/A/N generator communication.(U) The DDPU and A/N generator request access to the alphanumeric memory by the C-bus request line (CBRQS−) and the alphanumeric memory bus request line (MBRQS−), respectively. The RAM cannot be accessed by the C-bus and the alphanumeric A/N bus simultaneously. After the control logic receives either CBRQS− from the DDPU C-bus or MBRQS− from the symbol memory bus, the control logic latches up to accept only that particular bus, locking out the other until the next memory cycle. When a memory cycle is complete (either a write operation has been performed or valid output data is available for a read operation), an acknowledge (CBACK−) or (MBACK−) is sent to the DDPU or A/N generator, respectively, which ends the memory cycle. This allows the RAM to be accessed by either the DDPU or the alphanumeric generator, whichever makes the request first. No special signals are required for communication between the alphanumeric memory and the A/N generator other than MBRQS−, MBA00− thru MBA11−, the memory bus data (MBD00− thru MBD15−), and MBACK−.

c(U). Input address multiplexer.(U) A 12-bit address is required to access a memory location in the RAM, six bits for the column and six bits for the row. Two 6-bit bytes of the C-bus address or two 6-bit bytes of the A/N memory bus address are used to address the location in the RAM. The two 6-bit bytes are alternately selected through the input address multiplexer by the SELECTA and SELECTB control signals, which also select either the C-bus or A/N memory bus address. Each 6-bit address is transmitted alternately to the refresh address multiplexer to the RAM.

d(U). Alphanumeric memory refresh.(U) Because the RAM is a dynamic type, it requires a refresh cycle to retain its data. The 33 kHz oscillator provides the basic refresh cycle frequency to the control logic which, in turn, provides the resetting pulse (REFRESH SET) to the oscillator and the CLK frequency to the refresh counter used to supply the 6-bit refresh address. These six refresh address lines are cycled sequentially to all the row addresses of the RAM through the refresh address multiplexer. The refresh address multiplexer switches between the six refresh lines and the six ADDRESS lines which come from the input address multiplexer. SELECT REF− from the address select and control logic selects which address bus should be switched in. ADDRESS STROBE− enables the refresh address multiplexer and the input data multiplexer.

e(U). Data input and output.(U) The input data multiplexer was designed to switch between receiving data from the CBD− bus and from the MBD− bus, but the MBD− input is disabled and only CBD− bus data is accepted to store data in the alphanumeric memory RAM.

The tri-state line drivers are used to output the memory data from the alphanumeric memory RAM to the CBD− bus and the MBD− bus. When low, READ ENABLE 1− enables the CBD− bus drivers; when READ ENABLE 2− goes low, it enables the MBD− bus drivers.

3-300(U). COMMAND MEMORY − 5A2A5A21.(U) The command memory is a 4096-word by 16-bit (4K x 16) dual port RAM. It is the primary memory portion of the DDPU subsystem. The command memory is used to store all instruction data and display programs loaded in form the CTT 5A1. The only logic interconnections to the command memory are through the DDPU address, data and control buses (C-bus). For a detailed logic unit interconnection diagram, refer to Volume V, figure 5-525, sheet 16. The command memory circuit card assembly is physically identical to, and interchangeable with, alphanumeric memory 5A2A5A17 and symbol memory circuit card assembly 5A2A5A13. The function they perform in each card location is different. The command memory circuit card assembly consists of eight major circuits as shown in the signal flow diagram (Volume V, figure 5-52521).

a(U). Address select and control logic (U) The address select and control logic section contains the circuitry necessary to decode the 4-bit device address code (CBA12− thru CBA15−) and the circuitry to process the RAM memory address selection, the enable lines, and the acknowledge ouput (CBACK−). The following control signals are provided by the address select and control logic.

(1)(U). READ ENABLE 1 enables the tri-state line drivers to drive the C-data bus (CBD00− thru CBD15−) data from the RAM.

(2)(U). SELECTA and SELECTB select the C-bus address 6-bit bytes (CBA00− thru CBA05−) or (CBA06− thru CBA11−) to the input address multiplexer.

(3)(U). ADDRESS STROBE− enables the refresh address multiplexer and, with SELECTB, selects the input data multiplexer CBD− bus.

(4)(U). COLUMN ADDRESS STROBE− clocks in the high order address bits to the RAM.

(5)(U). ROW ADDRESS STROBE− clocks in the low order address bits to the RAM.

(6)(U). CHIP SELECT STROBE− enables the RAM access.

(7)(U). READ/WRITE− RAM read/write control when low, enables writing into RAM.

(8)(U). REFRESH SET− rests the 33 kHz oscillator one shot and provides the clock frequency to the refresh counter.

(9)(U). SELECT REF− selects which address should be switched in, either the refresh address or input address.

b(U). Command memory/DDPU communication.(U) The DDPU requests access to the command memory RAM through the C-bus request line (CBRQS−). After the control logic receives a CBRQS− from the DDPU and when the memory cycle is complete (either a write operation has been performed or valid output data is available for a read operation) a C-bus acknowledge (CBACK−) is transmitted back to the DDPU. This acknowledge signal ends the memory cycle.

c(U). Input address multiplexer.(U) A 12-bit address is required to access a memory location in the RAM, six bits for the column and six bits for the row. The two 6-bit bytes are alternately selected through the input address multiplexer by the SELECTA and SELECTB control signals. Each 6-bit byte is transmitted alternately to the refresh address multiplexer to the RAM

d(U). Memory refresh.(U) Because the RAM is a dynamic type, it requires a refresh cycle to retain its data. The 33 kHz oscillator provides the basic refresh cycle frequency to the control logic. This in turn provides the resetting pulse (REFRESH SET−) to the oscillator and the clock frequency to the 6-bit refresh counter used to supply the refresh address. The six refresh address lines from the refresh counters are cycled sequentially to all the row addresses of the RAM through the refresh address multiplexer. The refresh address multiplexer switches between the six refresh lines and the six address bus lines which come from the input address multiplexer. SELECT REF− from the address select and control logic selects which address bus should be switched in.

e(U). Data input and output.(U) The input data multiplexer was designed to switch between receiving data from the CBD− bus and from an auxiliary data bus. However, in this application there is no other bus. Only the CBD− bus data is used to store data in the command memory RAM.

The tri-state line drivers are used to output the memory data from the command memory RAM to the CBD− bus when READEN1−, from the control logic, goes low.

3-301(U). CONTROL UNIT − 5A2A5A22.(U) The control unit circuit card 5A2A5A22 (Volume V, figure 5-52522) manages the operation of arithmetic unit circuit card 5A2A5A23.

The control unit circuit card contains the repository of microinstructions which translate a main program instruction into a sequence of microinstructions.

The control unit circuit card receives main program instructions from the 16-bit data bus portion of the I/O bidirectional bus. Other inputs to the control unit are mainly feedback signals from the arithmetic unit. The control unit generates, as output sequences, 39-bit control words that are fed to the arithmetic unit circuit card.

The two circuit cards, the control unit circuit card and the arithmetic unit circuit card, constitute a microprocessor. They are identified together as the DDPU. The two cards function as the DDPU, a single entity.

a(U). Input to the control unit.(U) The principal inputs to the control unit are the CBD06− thru 15− lines of the data bus portion of the I/O bidirectional bus. The CBD06− thru 15− signals are written into the instruction register.

Other signals to the control unit are interrupt, overflow, and halt feedback signals (RHEPR−, RLEPR−, RLECL−, OFLPR−, OFLCL−, OVRFL+ and OPHLT−) that originate in the arithmetic unit circuit card 5A2A5A23; start signals MBA00−A thru MBA03−A that originate in the bus buffer and control circuit card 5A2A5A27; and general feedback signals CSIGN−, ZRDET+, ALB00−, AB01−, ALB15, ALA15, CRYOT+, ALF00 that originate in the arithmetic unit.

b(U). Instruction register.(U) The 10-bit instruction register holds an instruction received from the main memory program via the data bus.

c(U). Instruction decoding logic.(U) The instruction decoder translates the main program instruction held by the instruction register into the microinstruction sequencer address, which, in turn, holds the control memory starting address of the microinstruction set. The instruction decoder output is fed to the next microinstruction address multiplexer.

d(U). Next microinstruction address multiplexer.(U) The next microinstruction address multiplexer selects either the PMA00− thru 5− lines to be channeled through to the microinstruction sequencer or it selects the microinstruction sequencer output to be channeled through to control memory.

The next microinstruction address multiplexer also receives start signal NWSTR+; interrupt signals RPH1R− and RPL0R−; overflow signal OFLFF−; control signal F00FF−; and arithmetic unit feedback signals CSIGN−, ZRDET+, ALB00−, ALB01−, ALB15−, and ALA15−.

e(U). Microinstruction seqeuencer.(U) The microinstruction sequencer holds control memory addresses. The microinstruction sequencer is initially triggered by the decoded main memory instruction. Subsequently, the sequencer steps through the set of control memory addresses holding the microinstructions needed to implement a main memory instruction. The sequencer is a PROM (256 words by 15 bits) and a microprogram counter. The sequencer feeds its address output to the microinstruction address holding register.

f(U). Microinstruction address holding register.(U) The 15-bit microinstruction address holding register holds the output of the microinstruction sequencer for multiplexing through to the control memory.

g(U). Control memory.(U) The control memory is the repository for the microinstructions. Inputs to the control memory are the RMA00− thru 07− lines from the microinstruction sequencer. The control memory is a PROM (256 words by 33 bits). The control memory has a 33-bit microinstruction output that is fed to the microinstruction register/decoder logic.

h(U). Microinstruction register/decoder logic.(U) The microinstruction register is 40 bits long. Thirty-nine bits are used and 1 bit is not used. The 39 bits consist of the 33-bit microinstruction from control memory and the 6 bits BAMOC−, HLTRQ−, CURUN, ALA15−, ALF00−, CRYOT+. Thus, a 39-bit control word is fed by the control register to the arithmetic unit to operate the unit.

i(U). Start, interrupt, halt.(U) The program start interface register is activated by inputs MBA00−A thru MBA03−A, which originate in the bus buffer and control circuit card 5A2A5A27 and signals MSTCL−A and CRCLK−7. The output of program start interface register is NWSTR+, INLIZ−, and a line to the clock circuit. NWSTR+ is fed to the next microinstruction address multiplexer and INLIZ− is fed to the microinstruction register/decoder logic.

There are two levels of interrupt, high-priority interrupt and low-priority interrupt. There is a single-line bus, RPTH1, to enable high-priority interrupts. A single-line bus, RPTLO, enables low-priority interrupts. The two single-line buses feed the interrupt enable/holding register that feeds enabling signals to the high interrupt enable/control circuitry and to the low interrupt enable/control circuitry. Once enabled, the high interrupt enable/control circuit is activated by input RHEPR− from the arithmetic unit and generates RPHIR−. This is fed to the next microinstruction address multiplexer. Once enabled, the low interrupt enable/control circuit is activated by inputs RLEPR− and RLECL− from the arithmetic unit and generates RPLOR−. This is fed to the next microinstruction address multiplexer.

The program execution can be completely halted by the halt circuit, which receives inputs OPHLT− from the arithmetic unit and INFCH− from the microcontrol word. The halt circuit generates output HLTRQ− fed to the microinstruction register/decoder logic.

j(U). Overflow flip-flop.(U) The overflow flip-flop receives inputs OFLPR−, OFLCL− and OVRFL+ from the arithmetic unit and generates output OFLFF−. This is fed to the next microinstruction address multiplexer.

k(U). Timing.(U) The clock circuit provides timing synchronization for the control unit and the arithmetic unit. The clock circuit receives inputs CYCLE− and STOPF− from the microcontrol word, CBACK− from the control bus, and a start signal from the program start interface register. The clock circuit generates output CBRQS−, which is fed to the control bus with CLOCK+, CLOCK− and INRCK−.

Inputs to the circuit card, MSTCL−A and CRCLK−7 are also used for timing synchronization.

l(U). Miscellaneous.(U) Signals DMXS1+ and DMXS2+ come from the arithmetic unit. DMXS1 and DMXS2+ are channeled through a NAND gate. The NAND gate output DMXSJ+ is sent back to the arithmetic unit.

3-302(U). ARITHMETIC UNIT — 5A2A5A23.(U) The arithmetic unit circuit card (figure 5-52523) receives data from the I/O bidirectional bus into its register file. It performs arithmetic operations, logic operations, or transfer operations on the data in the register file. It dispatches the data from the register file via the I/O bidirectional bus to specific locations whose addresses may also be generated in the arithmetic unit.

Dispatching of unaltered data from source to destination is the most frequent operation performed by the arithmetic unit circuit card. For example, all data between the DPU and the CTT is channeled through the arithmetic unit circuit card for proper acquisition from a source location and proper dispatching to a destination location.

The arithmetic unit accepts input from the 16-bit data bus portion of the I/O bidirectional bus and from the 39-bit microcontrol word signals of the control unit. The arithmetic unit generates outputs to the 16-bit data bus and 16-bit address bus portions of the I/O bidirectional bus.

The operation of the arithmetic unit circuit card is directly managed by the control unit circuit card 5A2A5A22. The two circuit cards, the arithmetic unit circuit card and the control unit circuit card, constitute a microprocessor configuration. They are identified together as the DDPU. The two cards operate as a single entity.

a(U). Input/output bidirectional bus.(U) The 36-line I/O bidirectional bus is organized into a 16-line CBD00− thru 15− data bus, a 16-line CBA00− thru 15− address bus and a 4-line CBRQS−, CBACK−, CBWRT−, CBJKP− control bus. The I/O bidirectional bus is the immediate channel for data input to and data output from the arithmetic unit circuit card.

b(U). Data input path to register file.(U) All data operated on by the arithmetic unit must first be written into the register file. By using the DATA ENABLE signal to disable the D tri-state gates, the CBD00− thru 15− lines can channel data from the enabled data bus to the register file input multiplexer, which then switches them through onto the MUX00− thru 14− and CSIGN− lines feeding the register file.

c(U). Data paths within the arithmetic unit.(U) Data already written into one of the registers of the register file is transferred to another register in the register file. This is accomplished by disabling the data bus through its tri-state gates and by using the DATA ENABLE to enable the D tri-state gates. This channels the data via ALA00− thru 15− lines output from the register file into the CBD00− thru 15− lines input to the register file input multiplexer to be switched onto the MUX00− thru 14− and CSIGN− lines feeding the register file.

Data written into the different registers of the register file can be selected to be operands for the arithmetic and logic unit (ALU). The result from the ALU is channeled back into the register file. Thus one or two operands can be channeled into the arithmetic and logic unit via the ALA00− thru 15− lines and ALB00− thru 15− lines. The resultant data output from the ALU is channeled via the ALF00− thru 15− lines to the register file input multiplexer to be switched on to the MUX00− thru 14− and CSIGN− lines feeding the register file.

d(U). Register file input multiplexer.(U) The register file input multiplexer switches either CBD00− thru 15− lines or ALF00− thru 15− lines onto the MUX00− thru 14− and CSIGN− lines which are input to the register file.

The selection action of the register file input multiplexer is controlled by the DMXS0+ thru 2+ lines and DMXSJ+ line output from the control panel input multiplexer.

e(U). Control panel input multiplexer.(U) The control panel input multiplexer selects the input to the register file input multiplexer. The control panel input multiplexer receives five input signals, DMXC0+ thru DMXC2+, WRITE−, RBDEN−.

The control panel input multiplexer has the output signals DMXS0+ thru 2+ and DMXSJ+ which control the select action of the register file input multiplexer. The control panel input multiplexer also generates the DATA ENABLE signal which enables or disables the D tri-state gates controlling the data flow from ALA00− thru 15− to CBD00− thru 15−.

The control panel input multiplexer is clocked by CURUN+.

f(U). Sign logic.(U) The sign logic circuitry generates the algebraic sign for data input to the register file.

Inputs to the sign logic block are the signals MUX15− from the register file input multiplexer, OVERFL+ and OVERFL− from the overflow detector and CSNEN+ from the microcontrol word output of the control unit circuit card.

g(U). Register file.(U) The register file is a temporary holding area of information needed immediately for the operation of the arithmetic and logic unit.

The register file is physically composed of nine 16-bit registers which are then functionally organized as seven 16-bit words and one 32-bit word as shown in table 3-277.

The inputs to the register file are the MUX00− thru 14− lines and CSIGN− line. The outputs from the register file are the ALA00− thru 15− lines and the ALB00− thru 15− lines. Therefore, writing into the register file can only occur one register at a time, but reading out of the register file can happen two registers at a time.

The selection of registers to which information is written and registers from which information is read is controlled by the register file address multiplexers.

The selection of having the register file operate in a mode of 8-bit bytes is controlled by the MS byte or LS byte select logic circuitry.

h(U). Register file A, B, C, address multiplexer.(U) The register file A or B or C address multiplexer selects the register to be written into and selects the register(s) to be read from in the register file.

Inputs to the register address multiplexer come from the microcontrol word register of the control unit circuit card and from the output of the register file. The signals MPCA0− thru 2−, MPCB0− thru 2− and MPCC0− thru 2− are received from the control unit. The signals CBD00− thru CBD05− are received from the register output file and are delayed in the holding register for synchronization with other timing sequences. Multiplexing action is directed by the control unit control register signals MPRS0+ thru 3+.

Outputs from the register address multiplexer are fed to the register file to enable and disable the selected registers.

i(U). Most significant byte or least significant byte selector.(U) The MS byte or LS byte selector chooses the 8-bit byte mode of operation of the register file.

Inputs to the MS byte or LS byte selector are the control unit control register signals MPRENH+, MPRENL+, and CLOCK+ and the CURUN+ and RPCLK−A signals.

Outputs of the byte selector are the register file clock inputs to the register file.

j(U). ALU.(U) The ALU performs 32 operations.

Table 3-277 (U) Register File Organization (U)

Register	Word	Abbreviation	Word Length (BITs)
16	STACK POINTER	(S)	16
16	PROGRAM COUNTER	(P)	16
16	ACCUMULATOR0	(A)	16
16	ACCUMULATOR1 AND EXTENSION	(E)	16
16	ACCUMULATOR2 AND INDEX	(X)	16
16	ACCUMULATOR3 AND BASE	(B)	16
16	ADDRESS	(AR)	16
16 16	TEMPORARY	(T)	32 (2 x 16)

The 16-bit ALU is composed of four 4-bit ALUs and a look-ahead propagate and generate carry logic module.

Data inputs to the 16-bit ALU are the ALA00− thru 15− lines and the ALB00− thru 15− lines. Thus, the ALU can receive up to two operands at once.

The data output of the ALU, ALF00− thru 15− lines, are fed back to the register file.

The control inputs to the ALU managing the ALU operation are the control unit microcontrol word signals ALUS00+ thru 03+, CRYIM−, ALUMD+.

Operational status outputs of the ALU are the CRYOT+ signal (indicating a carry out), the ALF15− signal (indicating possible overflow), and the zero detect signal ZRDET+.

k(U). Overflow detector.(U) The overflow detector monitors for an overflow condition in the ALU output.

Data inputs to the overflow detector are the MSBs of the inputs to the ALU, ALA15− and ALB15− signals and the MSB output of the ALU, ALF15− as well as the ALU operational control signals ALUS2+ and ALUS3+.

Data output from the overflow detector OVRFL+ and OVRFL− are fed to the sign logic block and to the control unit circuit card.

l(U). Data output path of arithmetic unit circuit card.(U) Data to be output to the I/O bidirectional bus is available only from the file register.

Data can be channeled from a selected register via ALA00− thru 15− lines through the enabled (by DATA ENABLE signal) D tri-state gates onto the CBD00− thru 15− lines and thus onto the data bus.

Address data can be channeled from a selected register via ALB00− thru 15− lines through the enabled (by CYCLE- signal) A tri-state gates onto the CBA00− thru 15− lines and then onto the address bus.

m(U). Control input to arithmetic unit circuit card.(U) The operations of the arithmetic unit circuit card are managed by the 39-bit microcontrol word output by the 40-bit control register of the control unit circuit card. The control signals and their functions are as follows.

OPGEN−	Enable signal for interrupt, halt overflow 3 — 8 decoder
F00FF−, A15FF−, RBDEN−, WRITE−, DMXC0+, DMXC1+, DMXC2+	Control selection of register file input multiplexer.
CSNEN+	Contributes to sign logic circuitry.
MPRENH+, MPRENL+	Controls selection of most significant or least significant byte mode.
MPCA0−, MPCA1−, MPCA2−, MPCB0−, MPCB1−, MPCB2−, MPCC0−, MPCC1−, MPCC2−	Control selection of registers in register file.
MPRS0+, MPRS1−, MPRS2+, MPRS3+	Control selection of inputs.
CYCLE−	Controls A tri-state gates.
ALUS0+, ALUS1+, ALUS2+, ALUS3+	Control operation of ALU.
CRYIN-	Controls carry-in to ALU.
ALUMD+	Inhibits carry mode.

n(U). Interrupt, halt and overflow feedback to control unit.(U) A 3-to-8 decoder with input from the register file A-address multiplexer generates seven signals output from the arithmetic unit as feedback to the control unit. The seven feedback signals are RHEPR−, RLEPR−, RLECL−, OFLPR−, OFLCL−, OPRST− and OPHLT−.

o(U). General feedback to control unit.(U) The arithmetic unit signals ALB00−, ALB01−, ALB15−, OVRFL+, CSIGN−, ALA15−, CRYOT+, ZRDET+, and ALF00− are also output as feedback signals to the control unit.

p(U). Miscellaneous.(U) The signals DMXS1+ and DMXS2+ are output to the control unit to be fed through a NAND gate, whose output returns to the arithmetic unit as DMXSJ+.

3-303(U). BUS BUFFER AND CONTROL — 5A2A5A27.(U) The bus buffer and control circuit card interfaces with the DDPU and the peripheral devices via three main buses, with associated extended buses. The block diagram of figure 3-164 shows an overview of the bus relationships between the bus buffer and control circuit and the various modules. The extended buses increase the number of peripherals that the DDPU can communicate with (see table 3-278). The DDPU comprises circuit cards 5A2A5A22 and 5A2A5A23.

Reset and master clear circuit
Restart circuit
Tri-state bus driver circuits
DMA circuit
DDPU halt sensor circuit
LED circuit

a(U). Reset and master clear circuit.(U) The reset and master clear circuit consists of gating drivers and a power-up circuit. A 100 μsec delayed reset occurs when the system is initially turned on via the power up sense circuit. A reset occurs also when the bus buffer and control circuit receives signal OPRST− from DDPU control unit 5A2A5A22.

The reset gating driver output signal RESET− disables all tri-state drivers via the control enable gating circuit. Output CBRST− and EBRST− (master clear) go to the LEDs. Signal EBRST− goes to the controls interface 5A2A5A9. Output MSTCL−A sends a master clear signal to the DDPU control unit

b(U). Restart circuit.(U) The restart circuit consists of a start-up sequencer and a control switching circuit. A DDPU restart sequence is initiated when the input start-up pulse PRGMLDNMLOPN goes LOW. The reset pulse resets the MBA00−A thru MBA03 outputs which go to control unit 5A2A5A22 of the DDPU. The start-up pulse also resets all the peripherals. After the start-up pulse has returned to a HIGH state, the sequencer which operates in conjunction with the control switching circuit sequences through six states. These six states generate six 4-bit words via the control switching circuit on output lines MBA00−A thru MBA03. The sequencer is clocked by input signal VIDEOACTIVE− from timing generator 5A2A5A10. During the start-up sequence, the select line is held LOW. The six control words generated in sequence result in the following actions: resetting of peripherals, activation of the C-bus, activation of the E-bus, new start on the C-bus, new start on the E-bus, and switching to DDPU control. These six control words are sent to the DDPU which causes the DDPU to reset and fetch the contents of the NEW START ADDRESS via the new start flip-flop. The data bits of the NEW START ADDRESS from the new address drivers are interpreted as an address. The DDPU goes to this address location, which contains the first execution instruction for the DDPU and begins successive program executions. At the completion of the sequence cycle, all of the sequencer outputs remain HIGH until cleared by a new start pulse PRGMDNMLOPN. The new address bus drivers are disabled by a master clear ERBST− or a CBACK− pulse. The new address bus drivers will remain disabled until a new start pulse PRGMLDNMLOPN is received from asynchronous interface 5A2A5A8.

Table 3-278 (U). Bus Buffer Functions (U)

C-Bus/E-Bus information flow

Function	Address	Data	Control
1. Reset	Off	Off	Off
2. Restart	New Start Addr on Bus	N/A	N/A
3. Read Req. from DDPU	C-Bus ← E-Bus C-Bus	← E-Bus C-Bus	← E-Bus
4. Write Req. from DDPU	C-Bus ← E-Bus C-Bus	← E-Bus C-Bus	← E-Bus
5. Read DMA req. from DDPU	C-Bus ← E-Bus C-Bus	← E-Bus C-Bus	← E-Bus
6. Write DMA req. from DDPU	C-Bus ← E-Bus C-Bus	← E-Bus C-Bus	← E-Bus
7. DDPU Read	Off C-Bus	← E-Bus	Off
8. DDPU Write	Off C-Bus	← E-Bus	Off

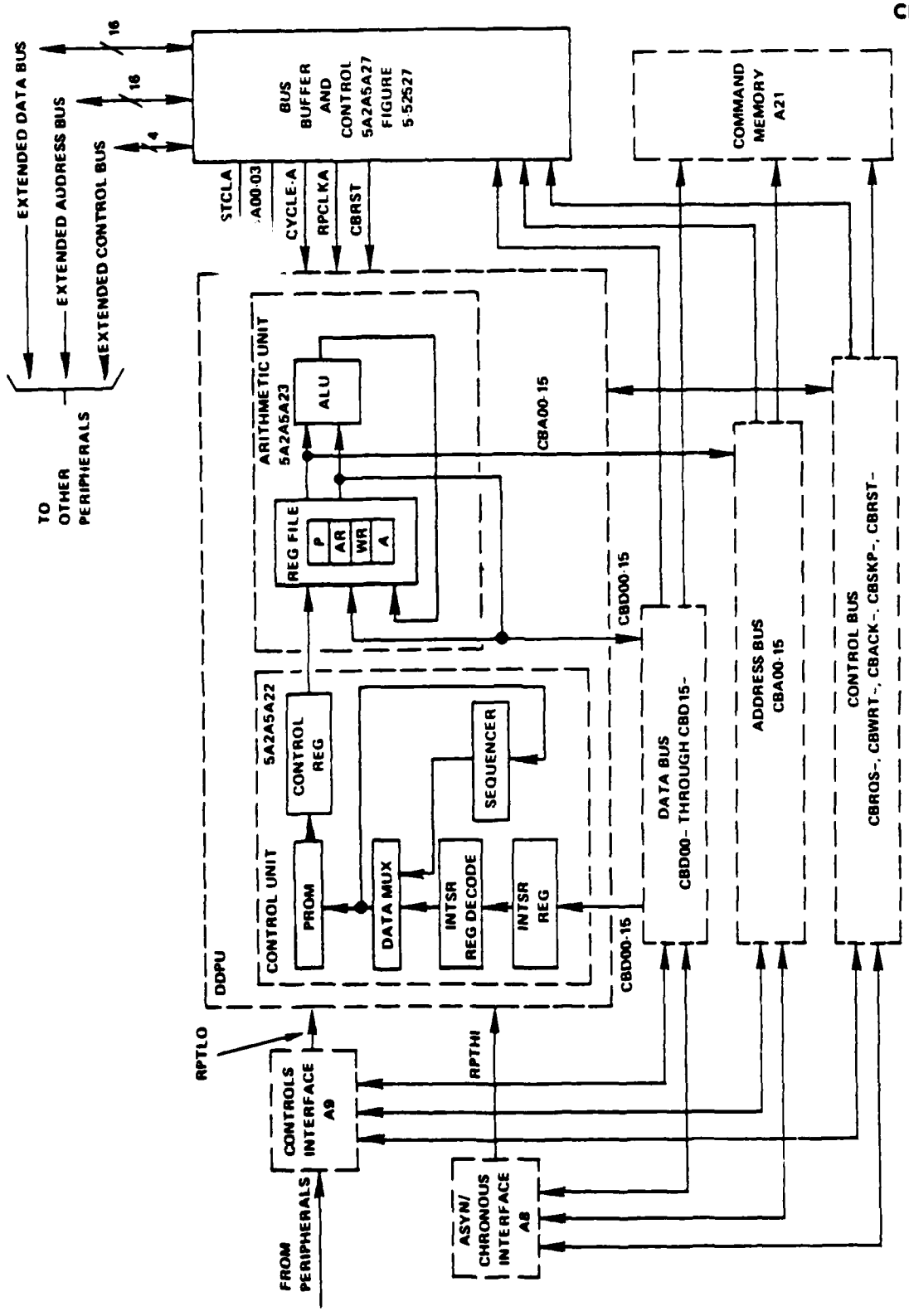


Figure 3-164 (U). Bus Buffer, Control and DDPU Block Diagram (U)

ERBST- or a CBACK- pulse. The new address bus drivers will remain disabled until a new start pulse PRGMLDNMLOPN is received from asynchronous interface 5A2A5A8.

One output of the start-up sequencer circuit and the video active signal combine in the AND gate to generate master clock control signal CRCLK−A, which is sent to control unit 5A2A5A22 of the DDPU.

Output signal RPCLK−A generates an interrrupt clock pulse to the DDPU during initial system start-up via the AU CLOCK driver AND gate. After start-up, RPCLK−A goes HIGH and the interrupt is disabled.

c(U). Tri-state bus driver circuits.(U) Upon completion of a reset and a new start sequence, control is relinquished to the DDPU. The bus buffer and control circuit now acts as an interface between the E-bus and the C-bus. The E-bus and C-bus include three sections: address, data and control. The address bus contains 16 address lines, EBA00 thru EBA15 and CBA00 thru CBA15 The data bus contains 16 data lines, EBD00, EBD15, and CBA00 thru CBD15, and the control bus contains five control lines, CBRQS−, CBWRT−, CBACK−, CBSKP−, and CBRST−. Address, data and control information are sent to and from the C-bus and E-bus via the bus buffer tri-state drivers. The bus drivers are controlled by the control enable gating circuit and the data enable gating circuits. The signals which control these drivers are listed in table 3-279.

The signals in table 3-279 determine the direction of information flow by disabling or enabling respective bus drivers. Table 3-280 lists the bus driver enable signals and the logic required to transfer information to or from the respective buses. The term LEFT means that information is going from the E-bus to the C-bus. The term RIGHT means that the information is going from the C-bus to the E-bus. The signals that control the direction of information flow are listed as internal logic signals.

Table 3-279 (U) Bus Driver Control Signals (U)

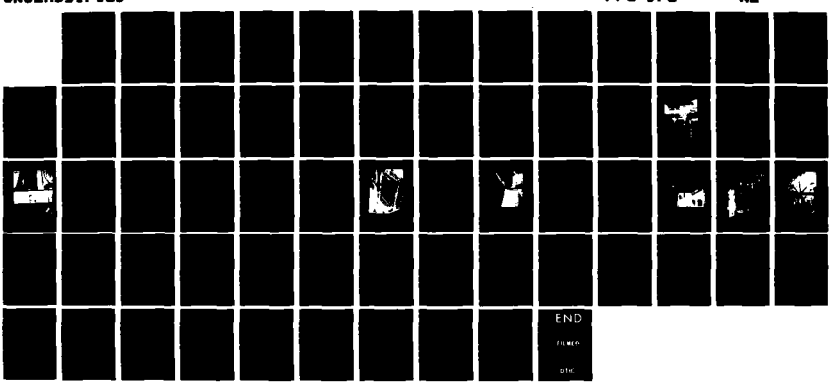
	Signal	Origin
A.	REGEN	Control enable gating circuit
B.	CURUN+	DDPU
C.	DMA REQ−	DMA flip-flop circuit
D.	RBDEN−	DDPU
E.	CBWRT−	C-BUS
F.	EBWRT−	E-BUS
G.	CBACK−	C-BUS
H.	EBACK−	E-BUS
I.	RESET−	Control enable gating circuit

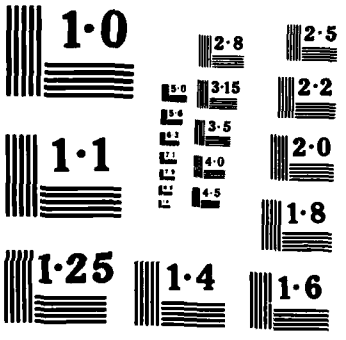
Table 3-280 (U) Internal Logic Signals (U)

	Internal logic signals	Logic required	Lines enabled
J.	ADDRESS ENABLE RIGHT+	$\overline{CI} + \overline{BI}$	EBRQS−, EBWRT−, EBA00−15
K.	ADDRESS ENABLE LEFT+	$\overline{IB}C$	CBRQS−, CBWRT−, CBA00−15
L.	SKIP, AKN ENABLE RIGHT+	$K\overline{E}$	EBSKP−, EBACK
M.	SKIP, AKN ENABLE LEFT+	$J\overline{H}$	CBSKP−, CBACK−
N.	DATA ENABLE RIGHT+	$KA\overline{D}+J\overline{E}+KF\overline{G}$	EBD00−15
O.	DATA ENABLE LEFT+	$KA\overline{D}+K\overline{F}+JF\overline{H}$	CBD00−15

AD-A158 515 MASS MEMORY STORAGE DEVICES FOR AN/SLQ-32(V)(U) NAVAL 2/2
SURFACE WEAPONS CENTER DAHLGREN VA L C TRIOLA
01 JUN 85 NSWC/TR-85-133 SBI-AD-F350 038

UNCLASSIFIED F/G 9/2 NL





Based on the logic in Table 3-177, the following functions are performed.

1. Read request from DDPU
   This is a FETCH. Address and control information are transferred from the E-bus to the C-bus. Data information is transferred from the C-bus to the E-bus.

2. Write request from DDPU
   This is a STORE. Address, control, and data information are all transferred from the E-bus to the C-bus.

3. Read request from DDPU/DMA
   This is used when the unit controlling the C-bus desires to fetch data stored on the E-bus. Address and control information are transferred from the C-bus to the E-bus. Data information is transferred from the E-bus to the C-bus.

4. Write request from DDPU/DMA
   This is used when the unit controlling the C-bus desires to store data onto the E-bus. Address, control and data information are all transferred from the C-bus to the E-bus.

5. DDPU read register
   Data stored in registers is transferred from the C-bus to the E-bus. Bus control drivers are OFF.

6. DDPU write register
   Data is stored from the E-bus into registers on the C-bus. Bus control drivers are OFF.

d(U). DMA circuit.(U) The DMA circuit allows the transfer of words between memory 5A2A5A21 and the peripheral devices. The DDPU operation is suspended during the execution of DMA. The bus buffer and control circuit supplies the circuitry to perform DMA transfers between the peripheral I/O devices and the local bus. Input signal CYCLE− from the control unit 5A2A5A22 of the DDPU simultaneously supplies a low pulse to the DMA flip-flop circuit and one input of the three input NAND gate. The second input to the NAND gate is from the new start flip-flop. The third input to the NAND gate is from the DMA− flip-flop circuit. When all three inputs are HIGH, a LOW pulse is generated on output line CYCLE−A which goes to the arithmetic unit 5A2A5A23 of the DDPU.

e(U). DDPU halt sensor circuit.(U) The DDPU halt sensor circuit consists of a one-shot delay circuit. The one shot delay circuit senses a DDPU halt via control line EBRQS− If a read or write request is not received by the DDPU within a given period of time, the DDPU is halted and LED indicator D25 turns on. The period of time or delay of the one shot delay circuit is determined by the time constants of the R-C network. Provisions are made on the card to alter the circuit with jumper wires, so that a reset or a master clear is performed when a DDPU halt is sensed.

f(U). LED indicators.(U) The LED indicators with their associated lamp drivers are shown in Volume V, figure 5-52527, sheet 2. The bus buffer and control circuit card contains 25 LED and 25 lamp drivers which monitor the state of various lines. Except for MP HALTED all of the LED indicators light when their respective lamp driver inputs go LOW. MP HALTED lights when the input to its lamp driver goes high. Table 3-281 lists the LED and the lines they monitor.

NOTE

Signals CBA00 thru CBA15 are tied physically to the E-BUS but functionally reflect the status of the C-BUS address.

Table 3-281 (U). Bus Buffer LEDs (U)

LED	Line monitored
DS1−DS16	CBA00 thru CBA15
DS17	CBRQS−
DS18	EBRQS−
DS19	CBACK−
DS20	EBACK−
DS21	CBRST−
DS22	EBRST−
DS23	CBSKP−
DS24	EBSKP−
DS25	MP HALTED

APPENDIX C

SHOCK AND VIBRATION REPORT

FROM THE USS NEW JERSEY

DEPARTMENT OF THE NAVY

NAVAL SURFACE WEAPONS CENTER
DAHLGREN VIRGINIA 22448

7342

8000.1
E53-JJY
OCT 1 1 1984

From: Commander, Naval Surface Weapons Center
To: Commander, Naval Sea System Command
(SEA-61W2)

Subj: FIRING ARC ENLARGEMENT STRUCTURAL TEST FIRINGS IN USS NEW JERSEY

Ref: (a) NAVSEA INST 9110.1 of 14 Feb 1980
(b) NSWC ltr N43:JJY:plt 8800/BB-62-1 of Oct 1982
(c) NSWC ltr N43:JJY:plt 8800/BB-62-2 of Nov 1982
(d) NSWC ltr N43:JJY:plt 8800/BB-62-3 of Feb 1983
(e) NSWC ltr N43:JJY:ph 8800/BB-62-4 of May 1983

Encl: (1) Firing Arc Enlargement Tests in USS NEW JERSEY (BB-62)

1. Structural test firings, reference (a), are conducted to confirm that a ship's structure and equipment are capable of withstanding the vibration, shock, gases, and blast effects of weapons firings. The tests are designed to place the maximum allowable firing effects on the shipboard equipment, including other ordnance. The tests are required on modernized BB-61 class ships due to extensive installations of new equipment, including the Close-in Weapon System (CIWS), SLQ-32(V)3 Electronic Countermeasures Set, and HARPOON and TOMAHAWK cruise missile systems.

2. NEW JERSEY previously conducted structural test firings in 1982 and 1983, references (b), (c), and (d). Turret I successfully completed the requirements of reference (a) during these tests. Turret II was restricted in train to prevent damage to the forward CIWS mounts. Turret III, due to an electrical problem, could not be trained forward of 55°-48'. Therefore, it was recommended that the firing arcs of Turrets II and III be restricted to prevent damage to the ship and equipment. As a result of the tests, an improved understanding of the blast tolerance of the CIWS and improved analytical models of the 16" gun blast pressure distribution were obtained. With the improved data, the present experiments to enlarge the firing arcs were designed. The experiments were conducted out of Panama on 30 April and 2 May, 1984.

3. The Turret II firings were designed to produce incident blast overpressures of 5.0 psi and 4.6 psi, respectively, on CIWS Mount 21 and the starboard SLQ-32 antenna. Strains were measured in Mount 21 and the SLQ-32, and the firing was to be stopped in the event of equipment damage or critical strains. Test design level overpressures, critical strains, and a damaged radome on the SLQ-32 all occurred on the final round from Turret II. The incident overpressure became excessive on the TOMAHAWK launcher as a result of the final round fired from Turret III.

4. The observed damage and instrumentation results provide a clear understanding of the capabilities and limitations of the main battery with respect to arcs of fire: Turret I is unrestricted and can be fired from any position allowed by the positive stops in the Turret. Turret II should abide by the recommended limits in reference (e) for routine engagements. These limit

Subj: FIRING ARC ENLARGEMENT TESTS IN USS NEW JERSEY (BB-62)

the left barrel to 125°-30', center barrel to 120°, and the right barrel to 114° (relative). The enlarged firing sector explored in this test can be used with caution. When firing from this sector the ship can expect self-inflicted damage that may cause temporary loss of capability for other types of warfare. This zone covers 125°30' to 138°, 120° to 134°-20', and 114° to 124° relative, for the left, center, and right barrels respectively. As shown in enclosure (1), firing Turret II from abaft of these values will probably cause serious structural damage to the forward CIWS mounts and SLQ-32 Electronic Countermeasures Set. The portside limits are symmetrical.

5. The caution zone for Turret III begins at forward of 46° relative and extends forward to 42° relative for the left barrel. The center and right barrels can be routinely fired from as far forward as 42°. Firing from trains farther forward causes the blast loads on TOMAHAWK Launcher No. 7 to exceed design limits. Although this did not damage the launcher during the present tests, it could damage missiles stowed in the launcher. Also a projectile could strike the fueling at sea outrigger.

6. Enclosure (1) describes the response of the ship and equipment and the damage that resulted from the tests. Highlights for major equipment items are below:

a. CIWS Mount 21. Strains measured in the barbette panel were in the range of failure observed in static laboratory tests, but the panel did not fail. There were numerous circuit breaker failures during the firings. The breakers were not damaged and could be reset to restore the system to full capability. The heat exchanger in the Port CIWS magazine pulled way from its mounting and flooded the magazine. The search radome rotated slightly due to 16" gun blast. Improved designs for the barbette panel, circuit breakers, and heat exchanger mounting are recommended. Such improvements could allow larger firing arcs and improved survivability of the ship and equipment.

b. SLQ-32(V)3 Electronics Countermeasures Set. The system was fully operational during the tests. Signals simulating threat emitters were injected and engaged during the firings. Numerous system faults occurred as a result of the firings, but the system always restored to full operation until round 11, when high voltage power supply 3A10 went down permanently. On round 13 the forward transmit radome was broken. The door latches and related electrical interlocks failed early in the tests. Strains well in excess of the endurance (fatigue) limit were measured in the outboard door rail. The AN/SLA-10B Blanker in the ECM equipment room nearly came loose from the bulkhead. The recommendations are to improve the mechanical design of the enclosure and its supporting framework. The radomes should be supported during blast loading. The internal damage to power supply 3A10 should be analyzed. The AN/SLA-10B Blanker should be relocated or shock mounted. The cause of intermittent disruption of ECM during gun fire, even when there is no mechanical damage, should be investigated.

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c. TOMAHAWK Armored Box Launchers. The incident blast on the final round exceeded the 10 psi design level for the launchers, but no significant damage was found. The after launchers were empty, so no conclusions can be drawn regarding the response of contained missiles.

d. HARPOON Missiles and Launchers. No significant damage resulted.

e. Stabilized Glide Slope Indicator (GSI). The GSI was found damaged after the test was completed. The damage is surprising in that an operating GSI had been thoroughly tested at the Dahlgren Laboratory at overpressures up to 8.6 psi and positive phase durations of 3 to 4 milliseconds. The overpressures on NEW JERSEY were in the range 1.02 to 2.56 psi and 3 to 4 milliseconds duration. It is recommended that the existing GSI be repaired and a protective cover be provided for the fresnel lense. If problems persist, an inadequate foundation may be the problem.

7. In summary, NEW JERSEY completed structural test firings to enlarge the allowable firing arcs of Turrets II and III. The blast overpressures and equipment responses agreed with predictions used to design the tests. The results show that firing in the new sectors should be done with caution, and may cause temporary loss of capability for other types of warfare. Firing beyond the new limits could cause serious damage to the ship and equipment. The data obtained were used to develop recommendations for corrective actions and modifications to increase the survivability of the new equipment and the ship.

F. B. Sandy

F. B. [illegible]
By direction

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FIRING ARC ENLARGEMENT TESTS IN USS NEW JERSEY (BB-62)

Enclosure (1)

FIRING ARC ENLARGEMENT TESTS IN USS NEW JERSEY (BB-62)

I. BACKGROUND

Structural test firings, reference (1), are conducted to confirm that a ship's structure and equipment are capable of withstanding the vibration, shock, noise, gases, and blast effects of weapons firings. The tests are designed to place the maximum allowable firing effects on the shipboard equipment, including other ordnance. The tests also provide data for developing future ship designs, alterations, and equipment installations. Structural test firings are required on reactivated BB-61 class ships due to extensive installations of new equipment, including the Close-in-Weapons System (CIWS), SLQ-32 (V) 3 electronics countermeasures system, and HARPOON and TOMAHAWK cruise missile systems.

The procedures for structural test firing of guns, 3-inches and larger, enclosure (2) of reference (1), require firings from the limits of train and elevation from each barrel of each mount during part 1 of the test. The procedures in part 4 of the test require firing at each "worst case" gun firing orientation. These firing angles are to be selected to impose the maximum stress from gun muzzle blast on selected antennae and equipment.

USS NEW JERSEY conducted structural test firings in October 1982 and March 1983, references (2), (3), (4), and (5). Turret I was fired from the limits of train and elevation and successfully completed the requirements for structural test firing. Turret II was fired from angles of train and elevation that applied 3.4 psi incident overpressure on CIWS Mount 21. This produced a reflected overpressure load of 7.5 psi on Mount 21, which was then believed to be the design limit pressure for the PHALANX system. Turret II was trained to 125°-30' and 114° for the left and right barrels, respectively, for these firings. The PHALANX mounts and the SLQ-32 antennae withstood the blast. However, the instructions require firing from the limit of train, which is 150° for Turret II.

NEW JERSEY's structural test firing test plan called for firing Turret III from a relative train of 46°-30'. On the day of the test there was a problem that prevented Turret III from being trained forward of 55°-48'. The firing angle of 46°-30' would have applied the design level load to CIWS Mount 23. The forward limit of train of Turret III was previously 30°. However, the reactivation program included installation of a Fueling at Sea Outrigger boom that creates an obstacle at 40°-18' relative train and 25°-03' elevation from the left barrel of Turret III. Further, a 10 psi design overpressure limit on the TOMAHAWK armored box launcher creates an interference for the forward train limit of Turret III.

During the previous structural test firings, reference (5), the forward CIWS mount withstood an overpressure of 3.40 psi and 6 milliseconds (msec) duration from the 16-inch guns in Turret II. The measured reflected overpressure was 7.5 psi. The SLQ-32 antenna withstood 3.0 psi from the same firing. The 5"/38

caliber guns in Mount 51 subjected the forward CIWS to an incident overpressure of 5 psi and 3 msec duration. The measured reflected overpressures averaged 9.81 psi. Since the forward CIWS system had withstood significantly higher overpressure from 5"/38 caliber guns, it was decided to design a set of 16-inch firings to attain the same overpressure values. Presumably the equipment would survive and the main battery firing arcs could be enlarged.

The approach for enlarging the main battery firing arcs was incorporated into the structural test firing test plan for USS IOWA, reference (6), and was scheduled for March 1984. In 1983 NEW JERSEY was assigned to the Eastern Mediterranean Sea to participate in operations off Lebanon. It was subsequently decided to accelerate IOWA's production schedule so that NEW JERSEY could be relieved at the earliest possible time. PCO IOWA became concerned that there might be too little time between the tests and deployment to correct possible damage. He suggested, reference (7), that the tests be performed in NEW JERSEY enroute to post shakedown availability (PSA) after being relieved by IOWA.

In April 1984 the situation in Lebanon stabilized to the point where NEW JERSEY could be withdrawn. IOWA's accelerated schedule remained in force. At the request of the Naval Sea Systems Command (NAVSEA), the Naval Surface Weapons Center, (NSWC) promptly made plans to shift the testing to NEW JERSEY. SEA-06A approved the 16-inch portion of reference (8) on 23 April. NSWC then promulgated the firing and instrumentation plan, Appendix A. The NSWC test team arrived in Panama on 26 April. The Turret II firings were completed on 30 April off Nicaragua and El Salvador. The instrumentation was shifted aft, and the Turret III firings were completed on 2 May off Mexico. The test team disembarked the ship upon arrival in Long Beach on 5 May.

II. TEST OBJECTIVE AND DESIGN

The objective of the test was to fire Turrets II and III from angles of train and elevation that apply criteria overpressure loads to critical equipment items. Successful completion of the tests would provide data for prescribing new, enlarged firing arcs for IOWA class main batteries. The firing was to be stopped in the event of excessive pressure loads (5.0 psi on CIWS, 4.6 psi on SLG-32) or damage to the PHALANX or SLQ-32, reference (8).

Figure 1 shows the overpressure on the track radome of Mount 21 from Turret II as a function of train. Three separate curves are required, because for a given train of the turret, each muzzle is at a different distance and angle from Mount 21. For starboard firings, the right barrel of the turret is always nearest the mount, and always produces the highest overpressure for a given train of the turret. The curves shown are for the maximum elevation, which is nominally 45° for each barrel. The 5 psi overpressure ordinate is shown on the drawing and is the final design value for the tests. Firing from lower elevations puts the barrels at different distances and angles from the mount. Therefore, a different set of curves results from each elevation.

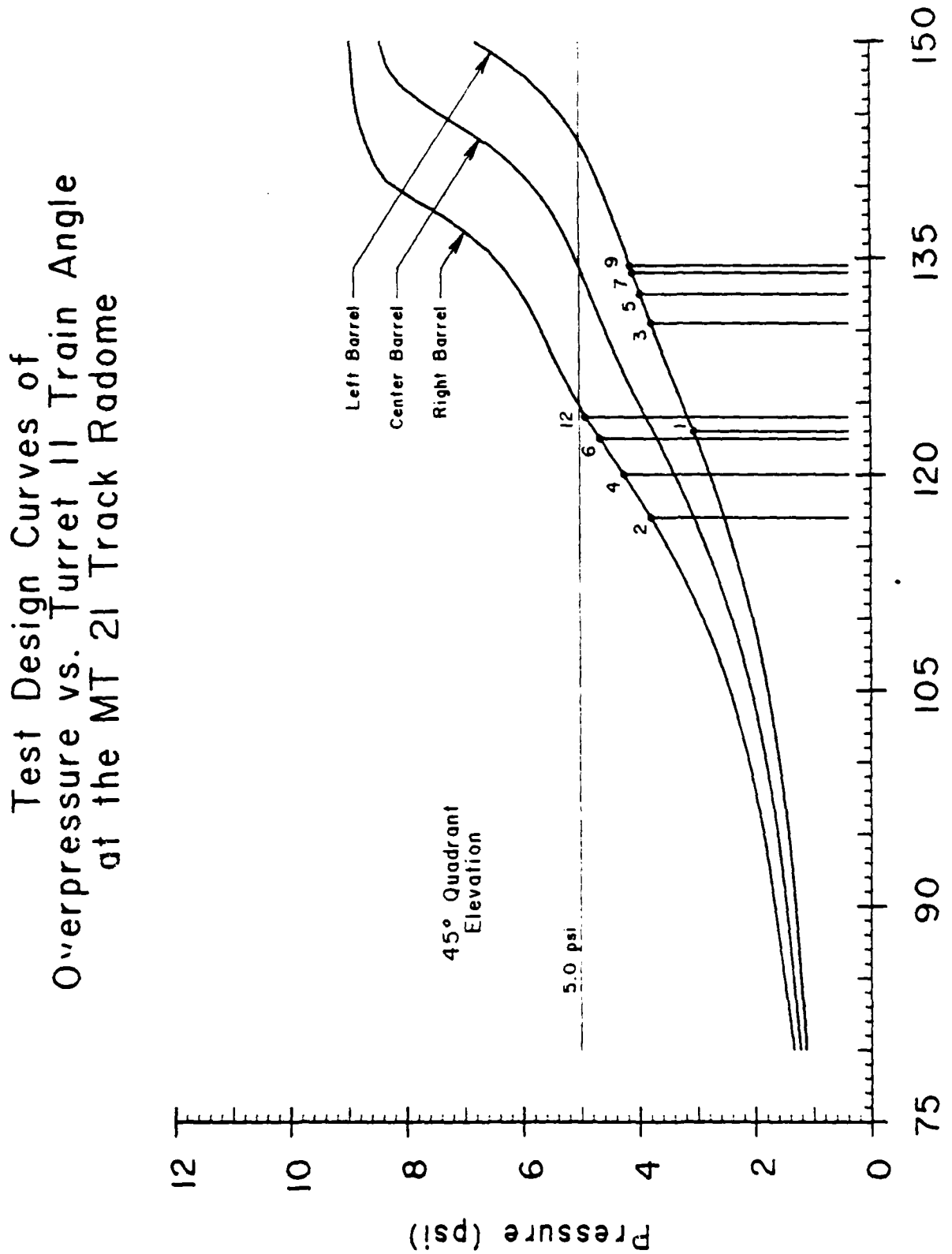

Test Design Curves of
Overpressure vs. Turret II Train Angle
at the MT 21 Track Radome
Left Barrel
Center Barrel
Right Barrel
45° Quadrant
Elevation
5.0 psi
12
6
4
2
1
3
5
7
9
Pressure (psi)
0
2
4
6
8
10
12
Train Angle (degrees)
75
90
105
120
135
150

FIGURE 1.

Thus, the 5 psi test design overpressure occurs at different relative trains for different elevations. The numbered points correspond to round numbers in the test plan.

Figure 2 shows parametric values of overpressure at Mount 21 that result from firing the left barrel of Turret II. Similar curves for the right barrel and SLQ-32 are shown in Figures 3, 4, 5, and 6. The center barrel of Turret II was not available for the test. Therefore, the firing plan consisted of alternate firings of the left and right barrels from positions of train and elevation that would incrementally increase the overpressure on Mount 21 to finally attain the critical value of 5 psi, as shown in Figure 2. The firings began at 135°-30' train, 45° elevation, which is an increase of 2 1/2° over the previous recommended firing limit. From there the firing proceeded to incrementally larger trains at the 45 degree elevation limit up to round 9. There the test design limit value for overpressure on the SLQ-32, to be discussed later, was attained. The final two rounds were fired from lower elevations to assure that a maximum overpressure load was applied to Mount 21 at the final train of the turret. As shown by Figure 5, the last three rounds apply the test design limit of 4.6 psi to the SLQ-32.

Figure 3 shows a similar set of curves for the starboard SLQ-32 antenna. The 16"/50 blast field creates rather pronounced "knees" in the curves in the range of 120° to 140°. In this range the increase in overpressure is very rapid with increasing relative train. This makes the train limit especially critical for this system. The test design value of 4.6 psi is also shown on Figure 2. As mentioned previously, this value was prescribed by NAVSEA as guidance in the design of the experiments. This barrel provides three rounds at the test design value for SLQ-32, one of which also applies the test design value to Mount 21.

The design of the right barrel firings is similar, except that the last three rounds apply the maximum value to Mount 21, and the last round also applies the maximum load to the SLQ-32 antenna.

Five additional rounds were held in reserve in case insufficient pressure loads were attained at critical equipment. These were not needed. The firing angles and round numbers are in shown Table I.

A special supplementary test plan for SLQ-32 is contained in Appendix A. The additional effort consisted of inserting simulated emitter signals in each side of the system with a signal generator, and engaging the simulated emitter with a combined transponder and repeater technique. In this way the ECM system was fully active during each firing. Complete system tests were run before and after the firings to assure the system was fully operational before the test, and to detect any damage or degradation of performance after the firings.

Until the present test, little was known about the tolerance of the SLQ-32 to blast. The antenna was subjected to a blast overpressure of 7.34 psi and 235 msec duration as a part of the field trial code named "Direct Course." The antenna sustained some damage, but could be repaired with spare parts. Previous main battery firings in NEW JERSEY had caused door latch failures. An improved latch was provided, but did not correct the problem. Petty Officers

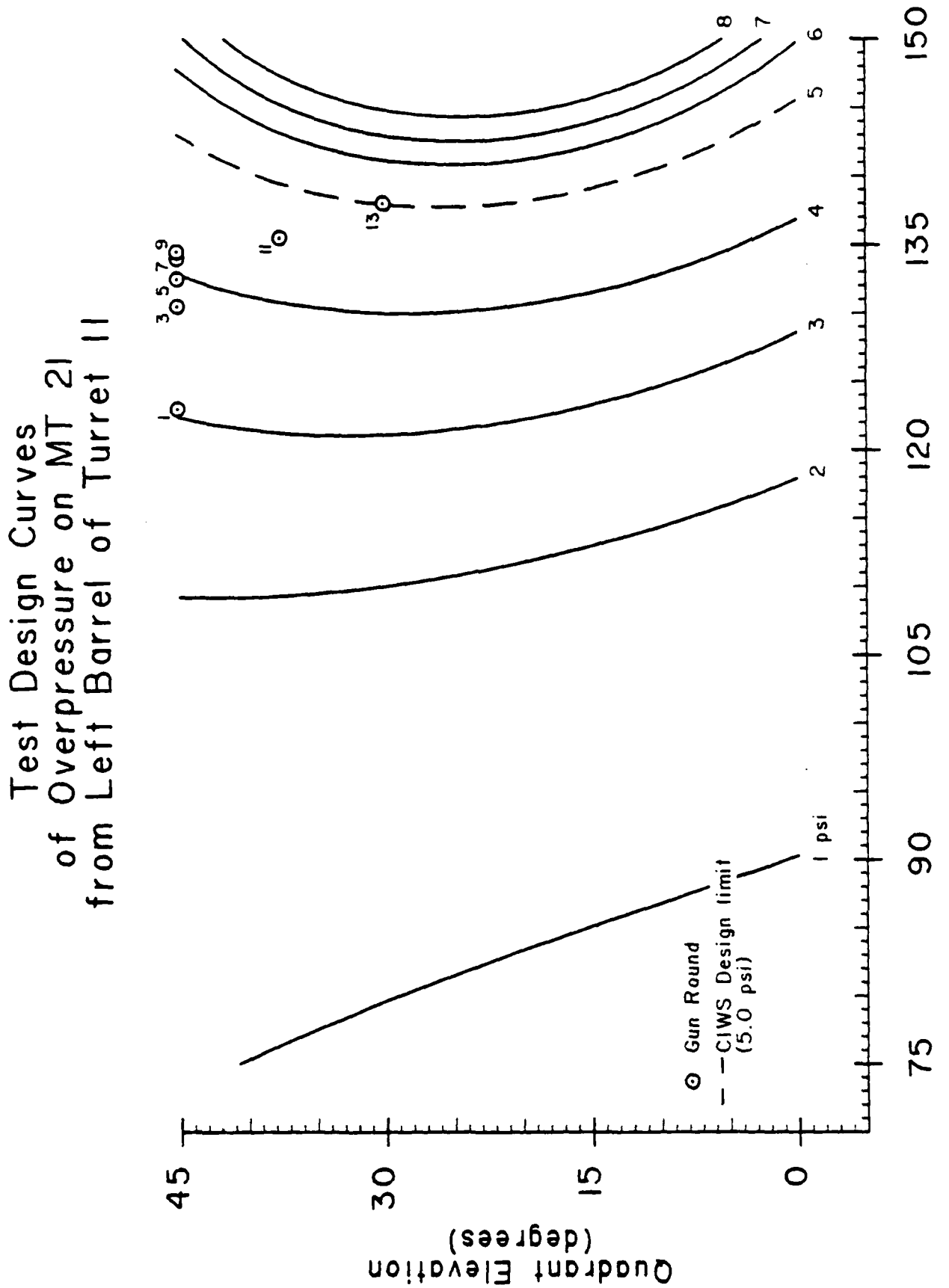

Test Design Curves
of Overpressure on MT 21
from Left Barrel of Turret II
Quadrant Elevation
(degrees)
45
30
15
0
75
90
105
120
135
150
Train Angle (degrees)
1 psi
⊙ Gun Round
— — CIWS Design limit
(5.0 psi)
1
2
3
4
5
6
7
8
9
11
13

FIGURE 2.

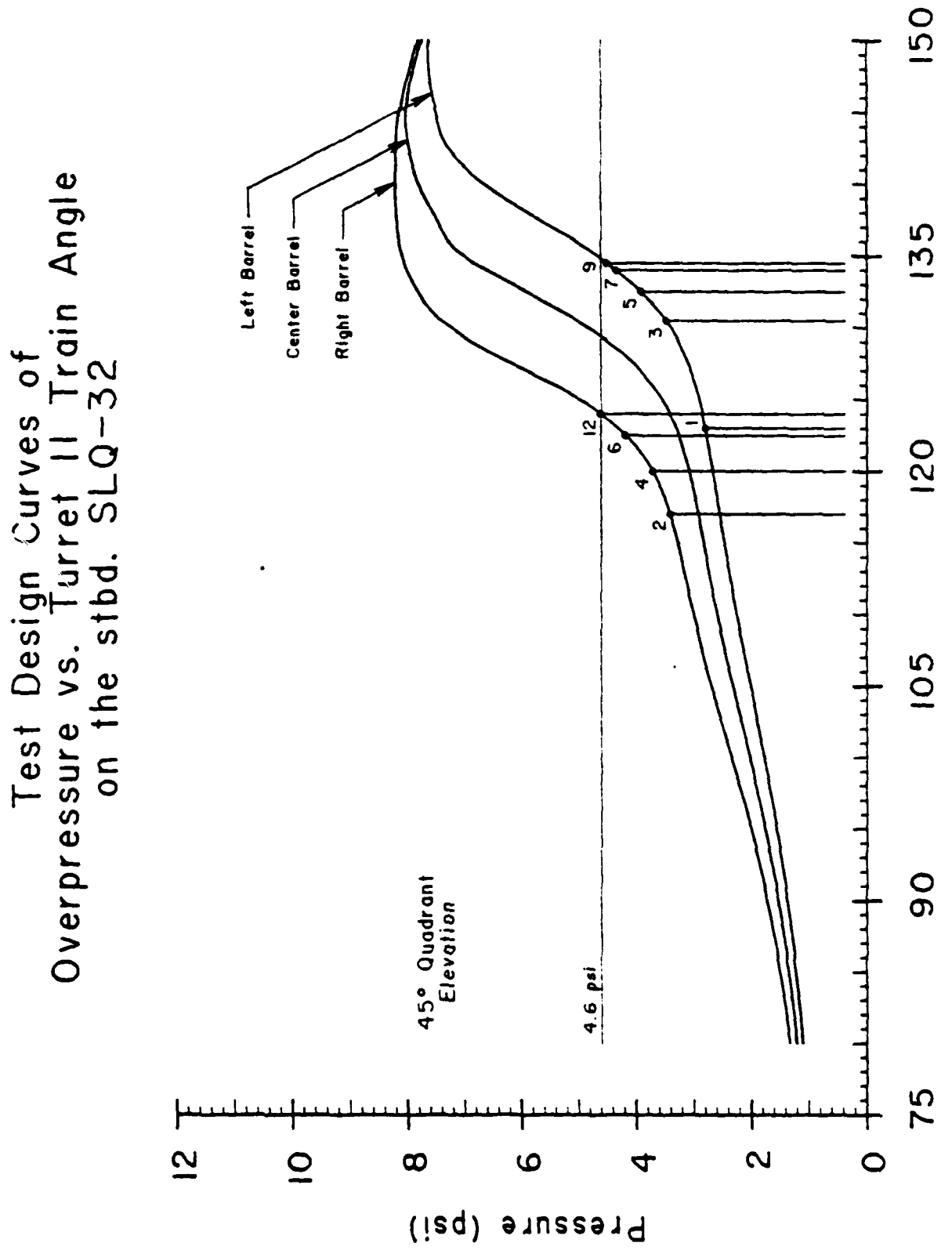

Test Design Curves of
Overpressure vs. Turret II Train Angle
on the stbd. SLQ-32
Left Barrel
Center Barrel
Right Barrel
45° Quadrant
Elevation
4.6 psi
12
6
4
2
1
3
5
7
9
Pressure (psi)
0
2
4
6
8
10
12
Train Angle (degrees)
75
90
105
120
135
150

FIGURE 3.

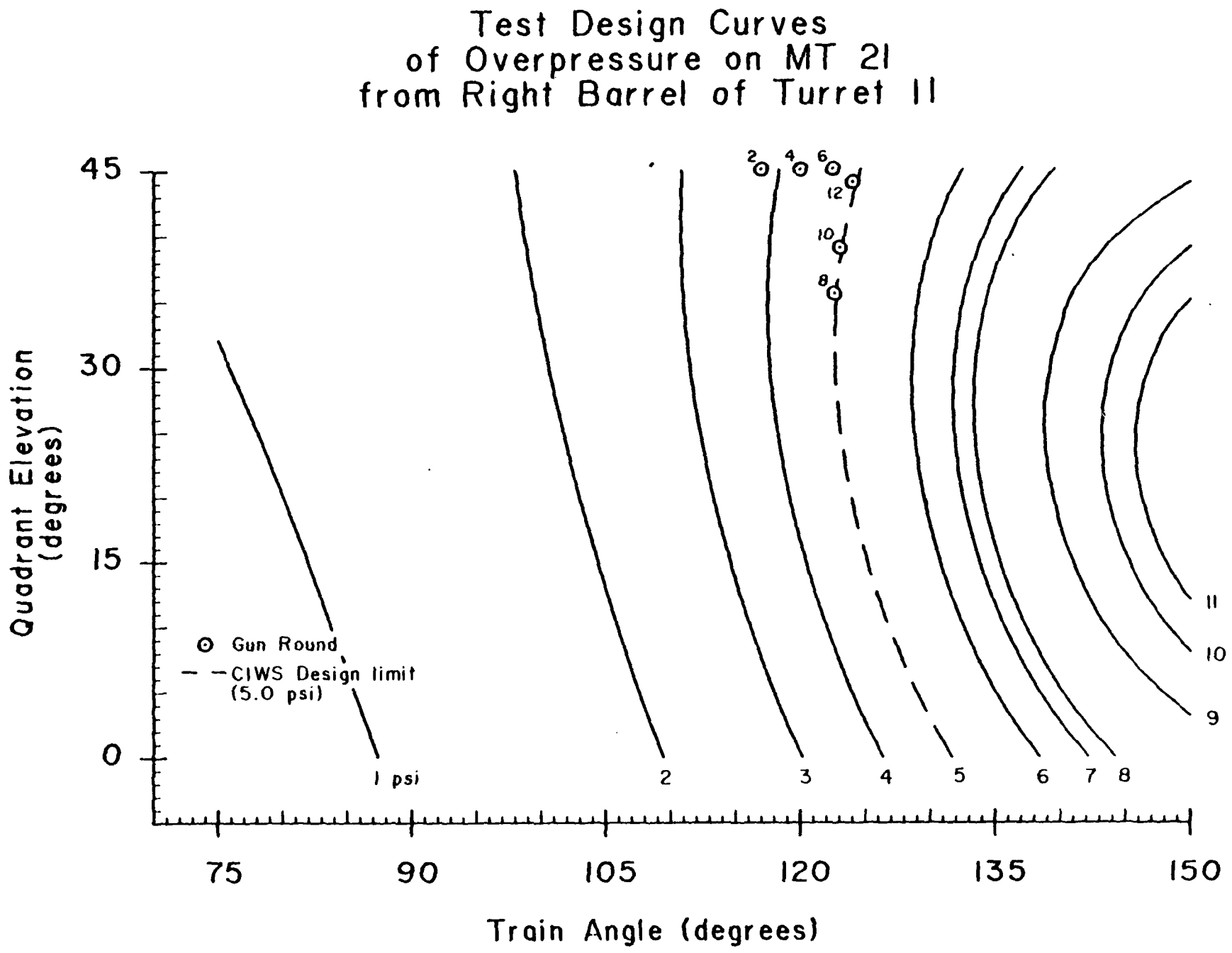

Test Design Curves
of Overpressure on MT 21
from Right Barrel of Turret 11
Quadrant Elevation (degrees)
45
30
15
0
Gun Round
CIWS Design limit (5.0 psi)
1 psi
2
3
4
5
6
7
8
9
10
11
12
75
90
105
120
135
150
Train Angle (degrees)

FIGURE 4.

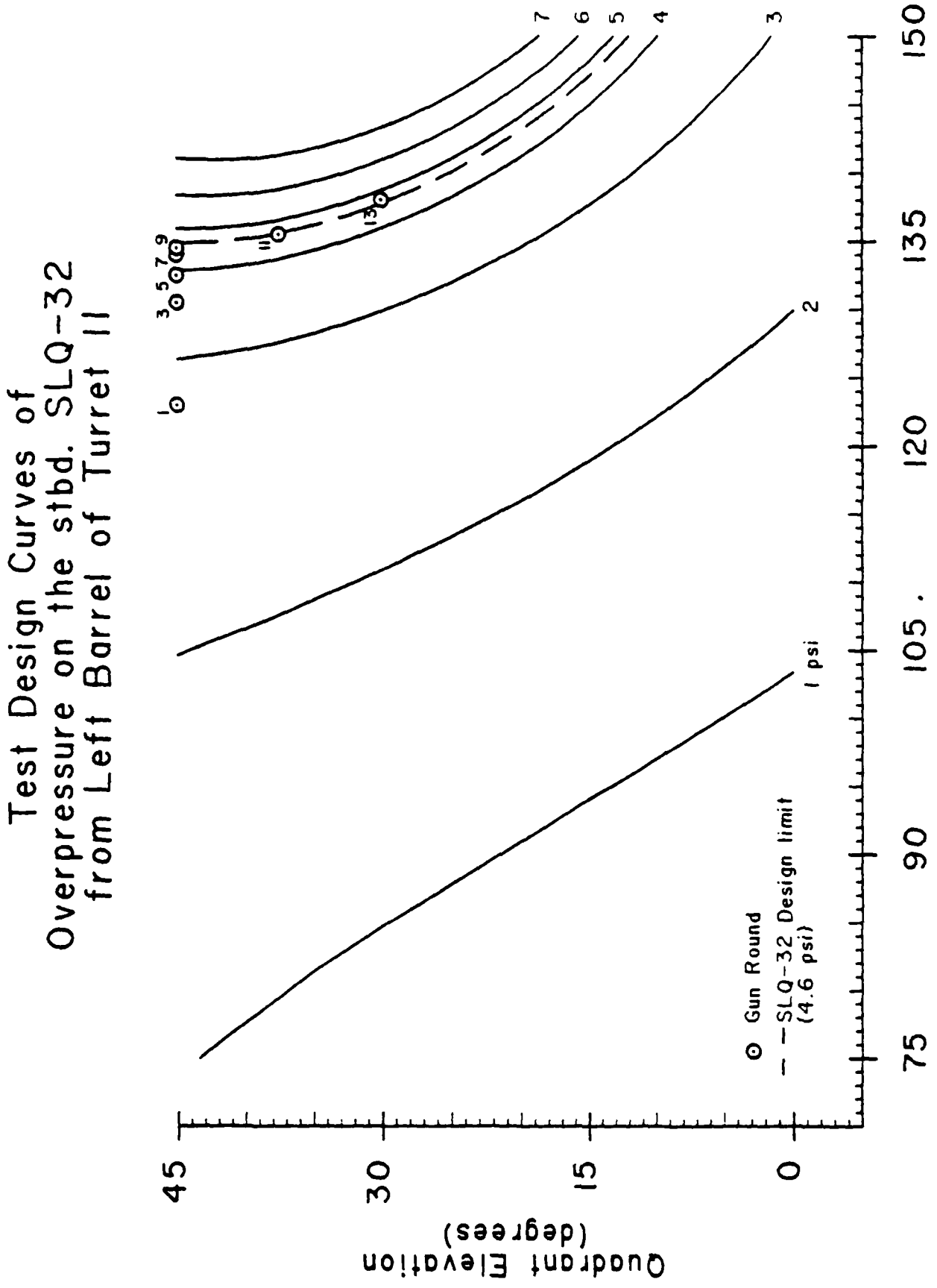

Test Design Curves of
Overpressure on the stbd. SLQ-32
from Left Barrel of Turret II
Quadrant Elevation
(degrees)
45
30
15
0
75
90
105
120
135
150
Train Angle (degrees)
1
2
3
4
5
6
7
1 psi
⊙ Gun Round
– – SLQ-32 Design limit
(4.6 psi)

FIGURE 5.

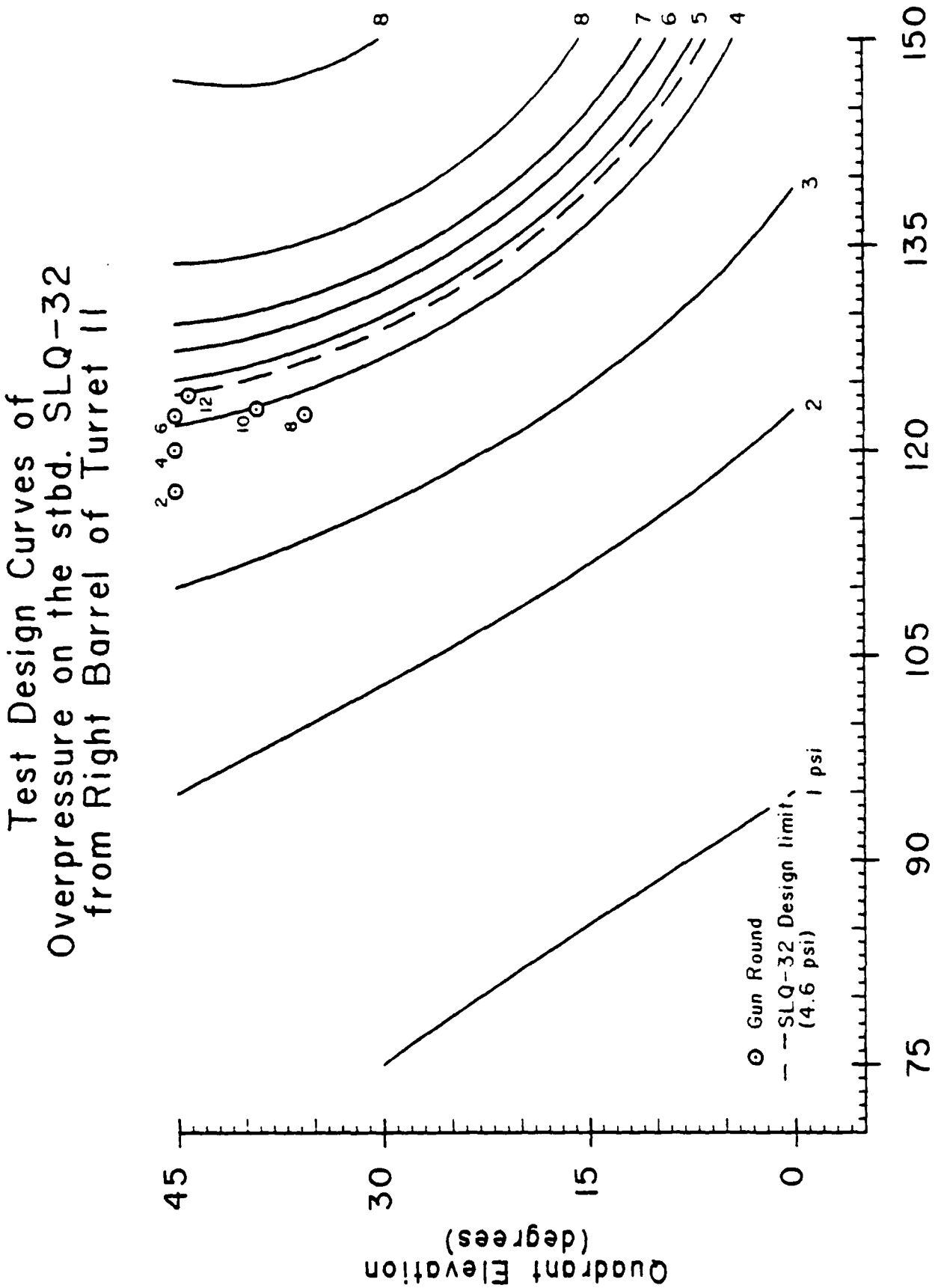

Test Design Curves of
Overpressure on the stbd. SLQ-32
from Right Barrel of Turret II
Quadrant Elevation
(degrees)
45
30
15
0
75
90
105
120
135
150
Train Angle (degrees)
⊙ Gun Round
– – SLQ-32 Design limit
(4.6 psi)
1 psi
2
3
4
5
6
7
8
8
2
4
6
8
10
12

FIGURE 6.

TABLE I

ROUND	TURRET	BARREL	TRAIN (deg)	ELEVATION (deg)	EXPECTED OVERPRESSURE MT 21 (psi)	SLQ-32 (psi)
1	2	L	128	45	3.5	3.2
2	2	R	117	45	3.8	3.5
3	2	L	130.5	45	3.7	3.6
4	2	R	120	45	4.3	3.8
5	2	L	132.5	45	4.0	4.0
6	2	R	122.5	45	4.6	4.1
7	2	L	134	45	4.1	4.3
8	2	R	122.5	35.5	5.	3.8
9	2	L	134.5	45	4.2	4.6
10	2	R	123	39	5.	4.0
11	2	L	135.5	37.5	4.5	4.6
12	2	R	124	44	5.	4.6
13	2	L	138	30	5.	4.6
14	2	R				
15	2	L				
16	2	R				
17	2	L				
18	2	R			MT 23	THWK NO.7
19	3	R	51	30	2.3	4.
20	3	R	46	30	2.4	4.7
21	3	C	51	30	2.6	5.
22	3	C	46	30	2.8	5.8.8
23	3	L	51	30	2.9	6.
24	3	L	46	30	3.2	7.2
25	3	L	46	25	3.2	7.6
26	3	L	46	22	3.1	7.8
27	3	L	46	18	3.	8.

responsible for the equipment in NEW JERSEY, reference (12), believed that the inadvertent latch opening problem could be alleviated through removal of small inspection ports in the rear of the enclosure, but this was not effective during the present tests. Negotiations between Naval Electronic Systems Command (NAVELEX) and NAVSEA engineers resulted in a limit value of 4.6 psi to apply to SLQ-32. This value was used to design the present experiments.

The design of the Turret III firings was much simpler. It was decided to design the firings to conclude at the forward limit value of 46° relative train in the original, approved, Phase II firing plan of reference (4). With the additional rounds available, a more cautious approach to the Fueling at Sea Outrigger and TOMAHAWK Launcher No. 7 was possible. Intermediate rounds at 51° relative train were therefore included . The final rounds were fired from 46 degrees as previously planned. Additional rounds from the left barrel at 46 degrees relative train and 22 and 18 degrees elevation were cancelled due to higher than expected overpressures at TOMAHAWK Launcher No. 7. The firing angles are shown in Table I.

III. Instrumentation Plan

The instrumentation system was a vital part of the test because the firings had to be stopped in event of excessive pressure loads or damage to the PHALANX or SLQ-32. The system employed sensors to measure the incident overpressure at Mounts 21 and 23, the starboard SLQ-32 antenna, TOMAHAWK Launcher No. 7, HARPOON Launcher No. 3, and the Glide Slope Indicator (GSI). Reflected pressures (the actual load created by the blast wave) were measured on the track radome, barbette panel, and electronics enclosure of Mount 21; the forward quadrant door of the SLQ-32 (starboard); the Fueling at Sea Outrigger; and TOMAHAWK Launcher No. 7. Strain sensors were installed on the Mount 21 barbette panel and starboard, forward corner post (outboard door rail) of the SLQ-32 antenna. Data from the sensors were played back, reduced, and plotted between rounds. This procedure assured that the blast loading was tracking the test plan, and provided structural response data that could be compared with predetermined failure criteria. Table 2 provides a summary of the channel number, applicable turret, purpose, and location of each instrument.

IV. Instrumentation Results

A. Pressure data, forward systems

Table 3 is a summary of the peak overpressure recorded by each sensor during the firings of Turret II. There is always a statistical round-to-round fluctuation in the blast overpressure that cannot be predicted. Therefore, one never expects precise one-for-one agreement between measured and predicted values. There is also variation in the measurements made at distances a few feet apart, as measured by P1 and P2. This is due to the complexity of the blast wave, which actually consists of many pressure waves traveling together superimposed on the main shock wave, and to round-to-round variation in the amount of propellant energy that is converted to blast. With the present 16-inch/50 caliber propellant, there is considerable combustion of propellant outside the gun barrel, which further contributes to flash, blast, and round-to-round variation.

TABLE 2. INSTRUMENTATION PLAN

INSTRUMENT CHANNEL NO.	TURRET	PURPOSE	LOCATION
P1	II	INCIDENT OVERPRESSURE AT MOUNT 21	RAILING ON SPONSON, FORWARD OF MOUNT 21
P2	II	INCIDENT OVERPRESSURE AT MOUNT 21, REDUNDANT	RAILING ON SPONSON, FORWARD OF MOUNT 21
P4	II	INCIDENT OVERPRESSURE ON SLQ-32	RAILING FORWARD OF ANTENNA ENCLOSURE, 18.4 FT STBD. OF SHIP CENTERLINE
P5	II	REFLECTED (SURFACE) OVERPRESSURE ON SLQ-32	SURFACE MOUNTED ON ANTENNA ENCLOSURE, 66" ABOVE DECK ON FWD QUADRANT DOOR
P6	II	REFLECTED OVERPRESSURE ON MOUNT 21 TRACK RADOME	SURFACE MOUNTED ON CYLINDRICAL SHROUD AT 19° RELATIVE TO SHIP, WEAPON STOWED. 144" ABOVE DECK
P7	II	REFLECTED OVERPRESSURE ON MOUNT 21 ELECTRONICS ENCLOSURE	SURFACE MOUNTED ON ELECTRONICS ENCLOSURE PANEL
P8	II	REFLECTED OVERPRESSURE ON MOUNT 21 BARBETTE PANEL	SURFACE MOUNTED AT CENTER OF PANEL
P10	III	INCIDENT OVERPRESSURE ON GLIDE SLOPE INDICATOR	RAILING STBD. OF GSI
P11	III	INCIDENT OVERPRESSURE ON TOMAHAWK LAUNCHER NO. 7	RAILING STBD. OF LAUNCHER
P13	III	INCIDENT OVERPRESSURE ON HARPOON LAUNCHER NO. 3	RAILING AFT OF LAUNCHER

TABLE 2. INSTRUMENTATION PLAN CON'T

INSTRUMENT CHANNEL NO.	TURRET	PURPOSE	LOCATION
P14	III	INCIDENT OVERPRESSURE ON CIWS MOUNT 23	RAILING AFT OF MOUNT 23
P17	III	REFLECTED OVERPRESSURE ON FUELING AT SEA OUTRIGGER	SURFACE MOUNTED ON ARM
P18	III	REFLECTED OVERPRESSURE ON TOMAHAWK LAUNCHER NO. 7	SURFACE MOUNTED ON LAUNCHER
P19	III	REFLECTED OVERPRESSURE ON TOMAHAWK LAUNCHER NO. 7	SURFACE MOUNTED ON LAUNCHER
P20	III	REFLECTED OVERPRESSURE ON MOUNT 23	SURFACE MOUNTED NEAR TRACK RADOME
S1	II	STRAIN RESPONSE OF MOUNT 21	SURFACE MOUNTED AT CENTER OF FORWARD PANEL, ATHWARTSHIP DIRECTION
S2	II	STRAIN RESPONSE OF MOUNT 21	SURFACE MOUNTED AT CENTER OF FORWARD PANEL, OBLIQUE DIRECTION
S3	II	STRAIN RESPONSE OF MOUNT 21	SURFACE MOUNTED AT CENTER OF FORWARD PANEL, VERTICAL DIRECTION
S4	II	STRAIN RESPONSE OF SLQ-32 ANTENNA ENCLOSURE	OUTBOARD DOOR RAIL, TRANSVERSE DIRECTION
S5	II	STRAIN RESPONSE OF SLQ-32 ANTENNA ENCLOSURE	OUTBOARD DOOR RAIL, VERTICAL (SPANWISE) DIRECTION
S6	II	STRAIN RESPONSE OF SLQ-32 ANTENNA ENCLOSURE	OUTBOARD DOOR RAIL, OBLIQUE DIRECTION
T1	II, III	TIMING	TIME MARK GENERATOR

TABLE 3. BLAST OVERPRESSURE AND STRAIN FROM TURRET NO. 2

CHAN.	LOCATION	1	2	3	4	5	6	7	8	9	10	11	12	13
P1	MT 21, Incident	nd	nd	nd	3.80	4.38	4.85	4.03	5.43	4.55	5.99	4.90	4.55	5.95
P2	MT 21, Incident	3.41	3.48	3.83	3.90	3.90	4.58	3.90	5.33	3.83	5.60	5.12	5.25	5.92
P4	SLQ-32, Incident	2.52	2.40	3.30	2.1	3.15	4.05	1.95	2.03	3.15	4.05	3.53	3.90	3.15
P5	SLQ-32, Reflected	8.15	8.62	8.15	8.70	7.94	9.74	9.06	8.24	9.06	9.51	9.51	9.29	8.38
P6	MT 21 Radome, Reflected	8.20	8.20	9.38	10.26	9.08	11.72	9.38	11.72	8.79	11.7	11.1	11.1	11.7
P7	MT 21 Elexencl, Reflected	3.04	3.95	4.56	3.30	4.56	5.58	3.45	5.07	4.06	4.82	5.07	5.07	5.07
P8	MT 21 Barbette Panel, Reflected	7.26	7.92	9.20	8.43	9.20	10.73	9.20	11.0	9.20	11.2	10.2	9.71	12.8
S1	MT 21 Strain, Athwartship	259	172	259	216	259	302	259	328	345	345	389	345	432
S2	MT 21 Strain, Oblique	840	980	980	1026	980	1166	980	1119	1073	1260	1119	1213	1260
S3	MT 21 Strain, Vertical	1411	1506	1694	1788	1741	2070	1741	1976	1694	2117	2070	2164	2089
S4	SLQ-32 Strain, Transverse	1626	1827	1870	1914	1914	2088	2001	1784	2045	2001	1870	2001	2001
S5	SLQ-32 Strain, Longitudinal	-276	-551	-349	-183	-276	-276	-230	-230	-230	-368	-138	-138	-257
S6	SLQ-32 Strain, Oblique	561	816	816	765	612	816	816	765	816	765	765	816	918

CIWS Principal Strain	1411	1521	1694	1788	1741	2070	1741	1976	1696	2117	2077	2165	2089
SLQ-32 Principal Strain	1633	1840	1871	1919	1933	2091	2003	1784	2049	2002	1875	2007	2001

The instruments P1 and P2, which redundantly measure the incident overpressure on Mount 21, are located between Mount 21 and the muzzles of the barrels in Turret II, Figure 7. When allowance is made for the decay in overpressure from the instruments to Mount 21, the agreement between the planned overpressure and the actual overpressure is very good. The measured data are plotted against predictions for actual locations of the instruments in Figure 8. These are actual plots made aboard the ship. Good tracking between P1 and P2 and the predicted values assured that the loading of Mount 21 was proceeding according to the plan.

The instrument P4 measured the overpressure incident on the SLQ-32, Figure 9. These data show that the test design criteria values were not being exceeded. The data are lower than predicted and do not correlate well with the reflected pressures measured by P5. It is believed that this is partially due to interference with the blast wave propagation due to very strong winds and turbulence in the atmosphere high on the ship. The ship was underway making 21 knots at the time of the test; this is not accounted for in the predictions for the SLQ-32 location. Round 13 caused a rupture of the starboard forward quadrant transmitter radome. The incident overpressure was 3.15 psi for this round. The incident overpressure was higher on previous rounds. Evidently, internal damage to the radome accumulated to the point where round 13 finally caused a visible failure. Because the test design objective had been obtained for Mount 21, and damage had occurred in the SLQ-32, testing with Turret II was complete at round 13.

B. Strain data

Strain gauge rosettes were mounted at the center of the forward barbette panel of Mount 21, Figure 7, and on the starboard forward corner post (outboard door rail) of the SLQ-32, Figure 10. Strain rosettes measure strain in three independent directions. For plane stress, as in a surface, the strain must be measured in three independent directions in order to resolve the principal directions and principal strains. The principal directions are directions in which the state of stress is pure tension or compression (no shear). The largest stress is always in a principal direction and is the stress that must be compared to the yield stress of the material. It is known from analysis and static tests that maximum strain in the barbette panel occurs on the surface at the center of the panel. It was not obvious, or known from any analysis, where the maximum strain would occur in the corner post of SLQ-32. The corner post was selected for instrumentation because it supports the closure latches that had a failure history, and it appeared that the forward corner post would carry a large strain due to blast waves arriving from the direction of the 16-inch gun muzzles. The instrument was located at midspan of the post, which would normally be the longitudinal section with the largest bending strain. Apparently good strain data were measured for each round. The strains correlate well with the reflected overpressure data measured at each system, Figures 11 and 12. The principal strains computed from S1 through S6 are also tabulated in Table 3. It is also clear that the strains measured are approaching critical values in each of the structures. There is more discussion of the strain data in the following section of this report.

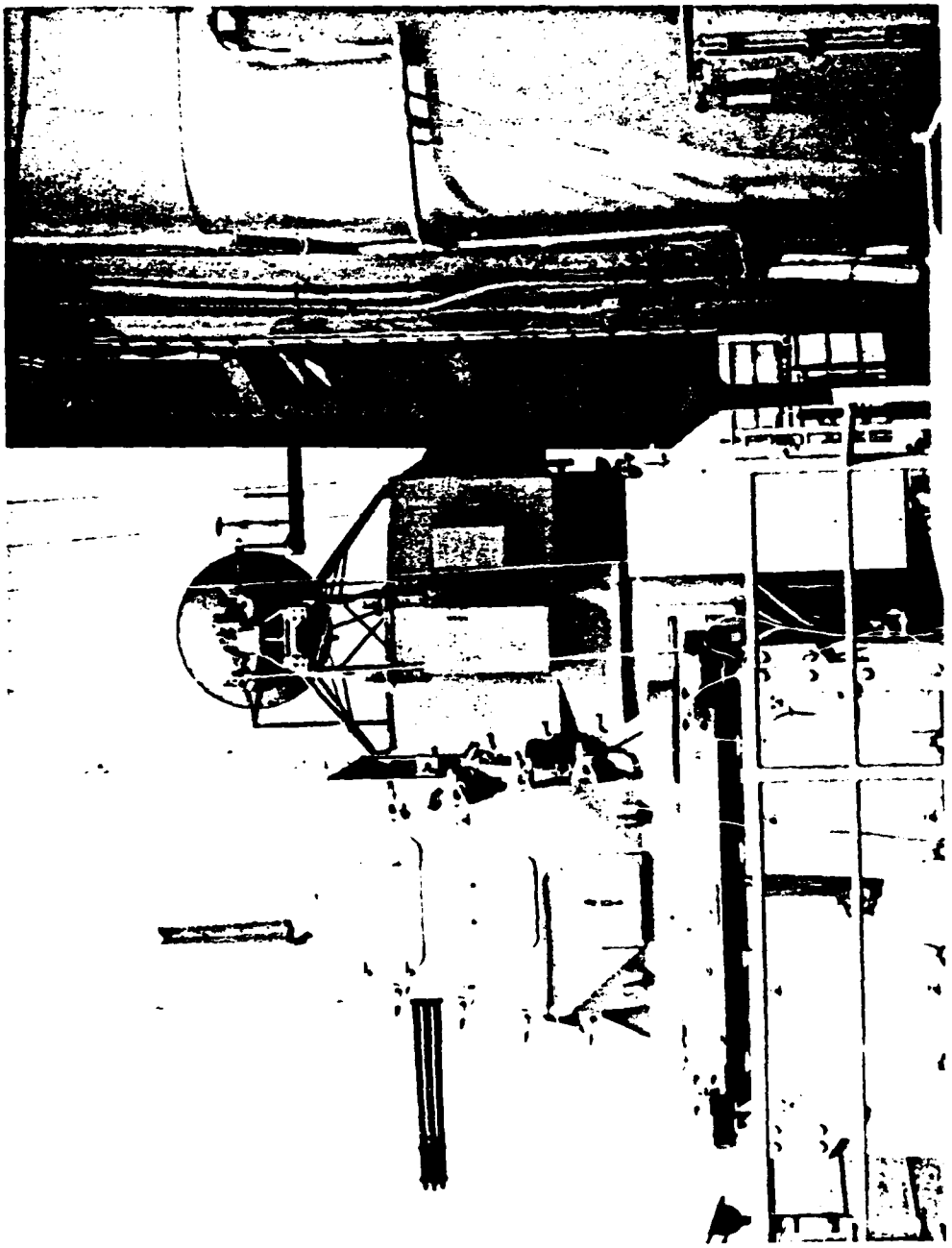


FIGURE 7. CIWS MOUNT 21 INSTRUMENTED FOR STRUCTURAL TEST FIRING. P1 AND P2 MEASURED INCIDENT OVERPRESSURE FROM TURRET II, P5, AND P6 MEASURED REFLECTED OVERPRESSURE ON BARBETTE PANEL AND SHROUD, RESPECTIVELY.

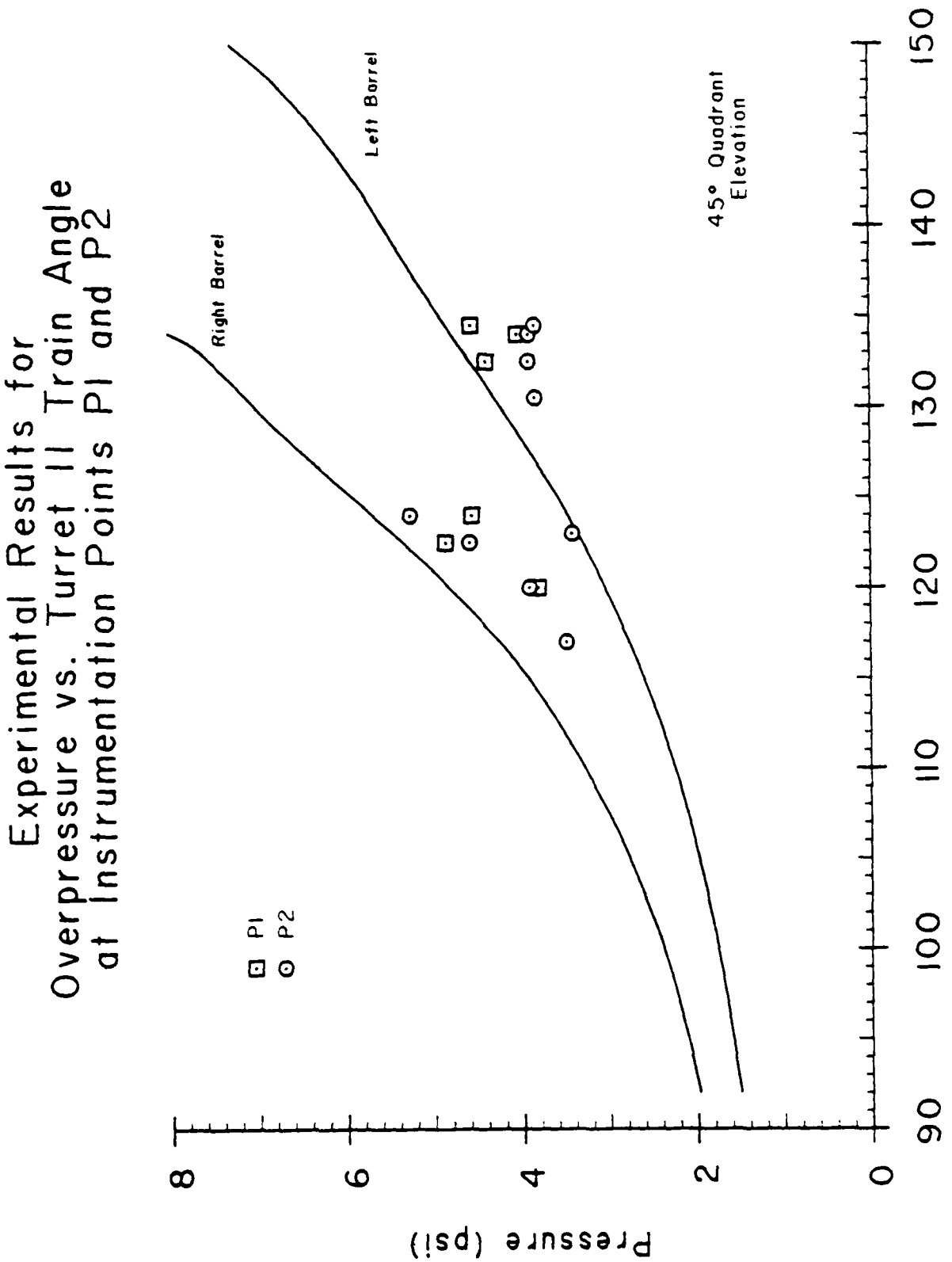

Experimental Results for
Overpressure vs. Turret II Train Angle
at Instrumentation Points P1 and P2
Right Barrel
Left Barrel
45° Quadrant
Elevation
P1
P2
Pressure (psi)
Train Angle (degrees)
0
2
4
6
8
90
100
110
120
130
140
150

FIGURE 8.

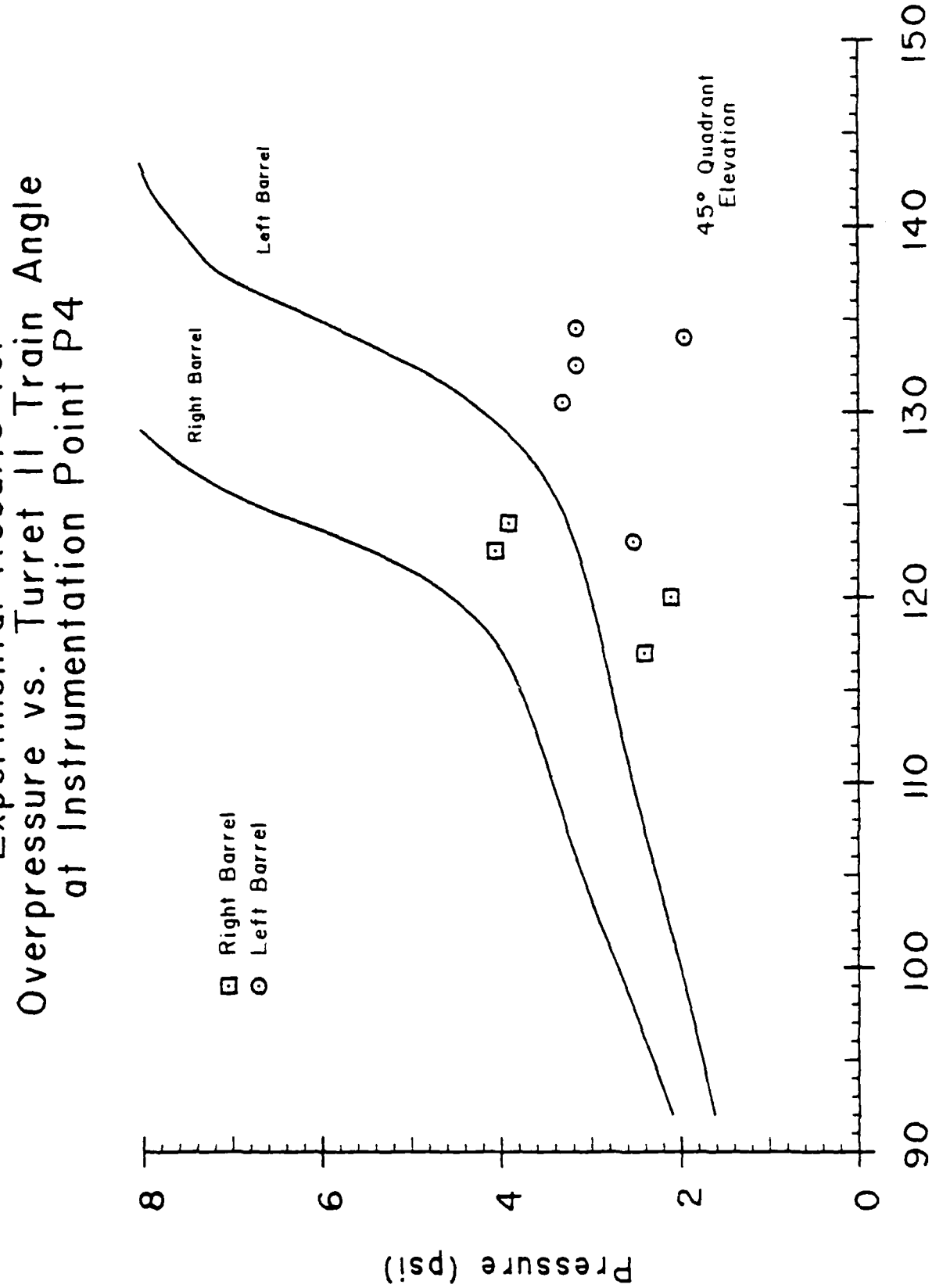

Experimental Results for
Overpressure vs. Turret II Train Angle
at Instrumentation Point P4
Right Barrel
Left Barrel
Right Barrel
Left Barrel
45° Quadrant
Elevation
Pressure (psi)
0
2
4
6
8
90
100
110
120
130
140
150
Train Angle (degrees)

FIGURE 9.

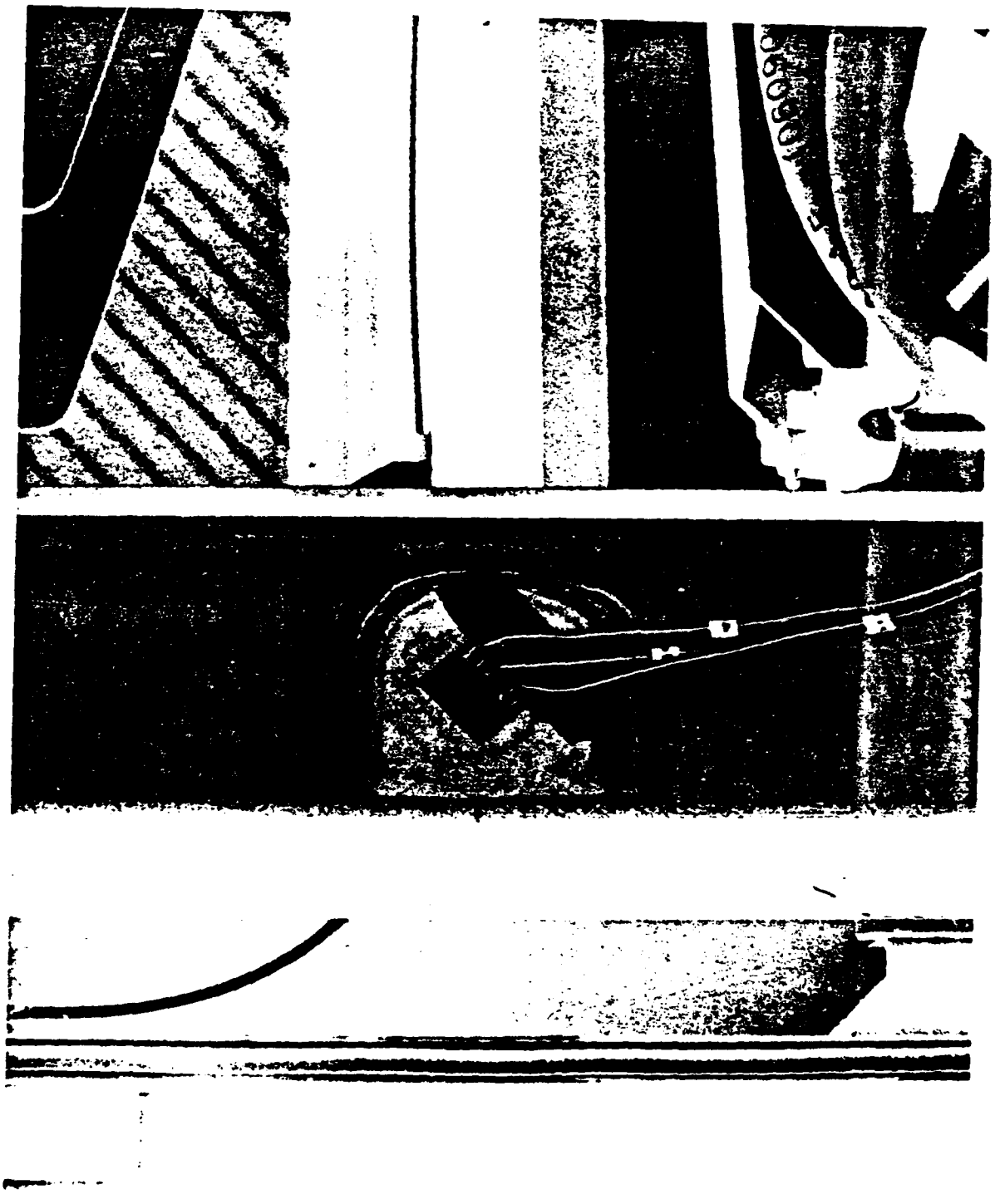


FIGURE 10. THREE-ARM STRAIN ROSETTE INSTALLED ON OUTBOARD DOOR RAIL OF SLQ-32 ANTENNA

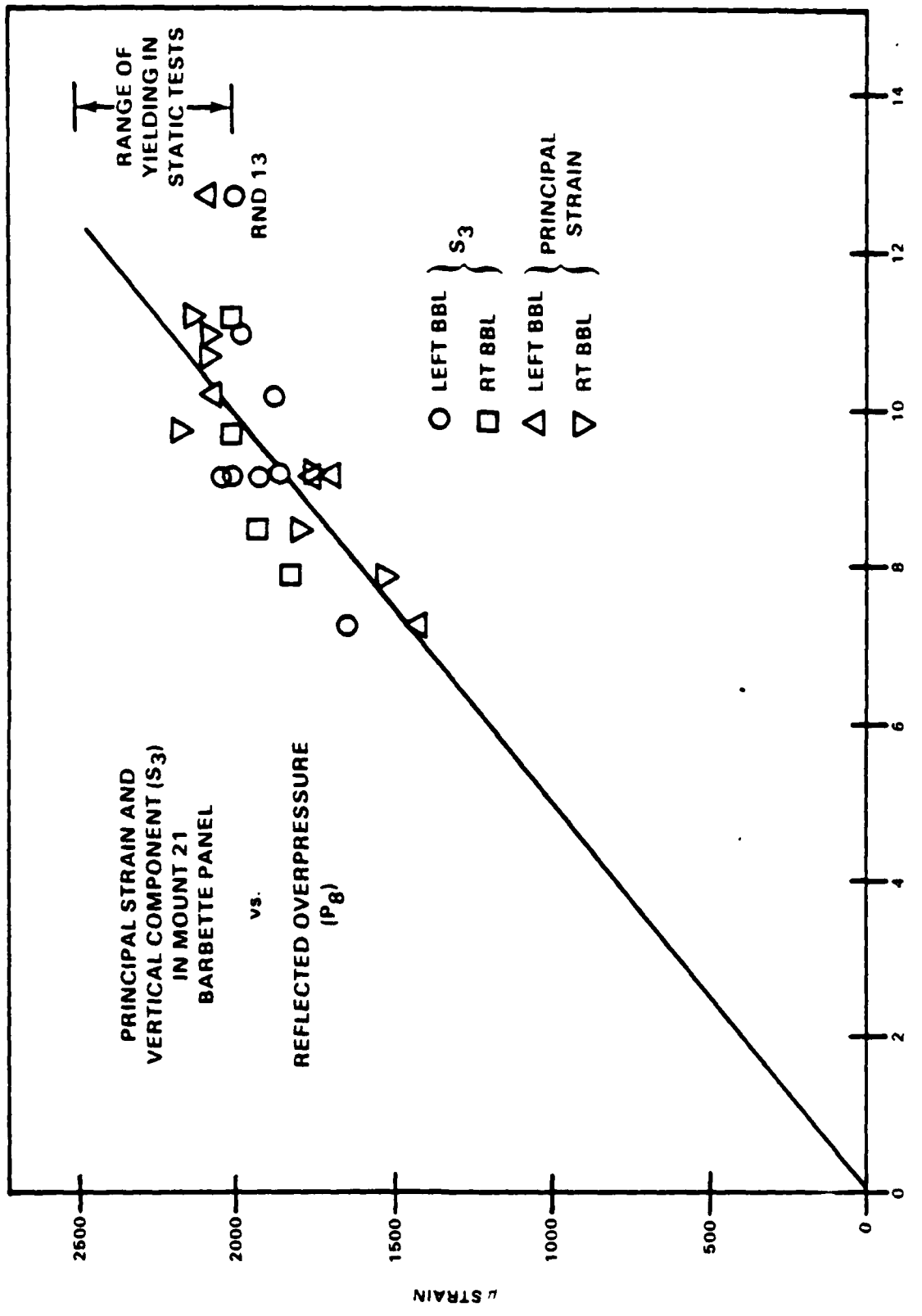

PRINCIPAL STRAIN AND VERTICAL COMPONENT (S_3) IN MOUNT 21 BARBETTE PANEL
vs.
REFLECTED OVERPRESSURE (P_8)
RANGE OF YIELDING IN STATIC TESTS
RND 13
LEFT BBL
RT BBL
S_3
LEFT BBL
RT BBL
PRINCIPAL STRAIN
μ STRAIN
2600
2000
1500
1000
500
0
0
2
4
6
8
10
12
14
$\Delta P_r (P_8)$ (psi)

FIGURE 11.

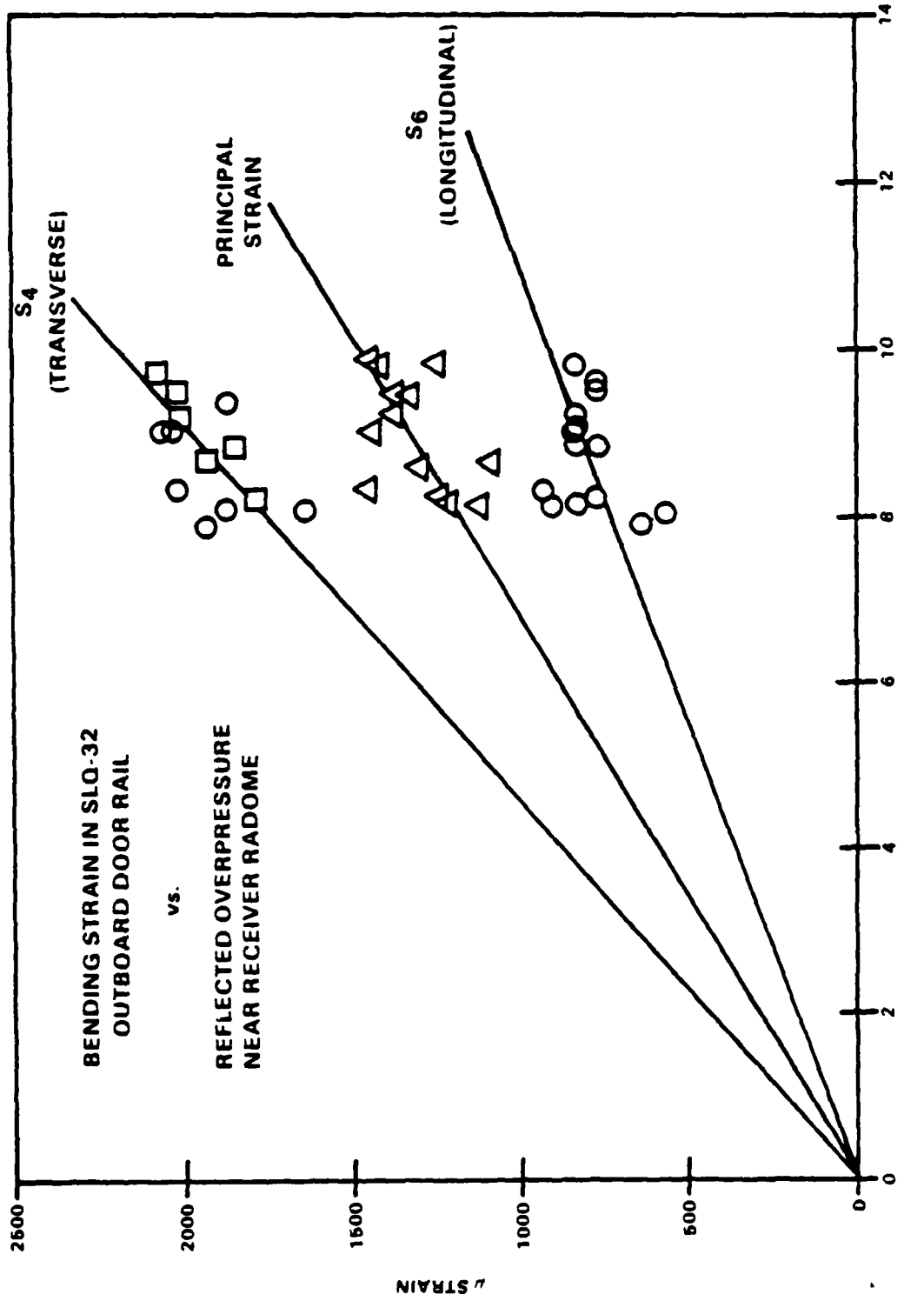

BENDING STRAIN IN SLQ-32
OUTBOARD DOOR RAIL
vs.
REFLECTED OVERPRESSURE
NEAR RECEIVER RADOME
S4
(TRANSVERSE)
PRINCIPAL
STRAIN
S6
(LONGITUDINAL)
μ STRAIN
2600
2000
1500
1000
500
0
0
2
4
6
8
10
12
14
ΔPr (P6) (psi)

FIGURE 13

C. Blast pressures, aft

Table 4 summarizes the blast pressures measured from firing Turret III. The pressure measured by instrument P11 on round 25 was higher than expected. From this measurement, and the known decay rate in overpressure with distance from the instrument to TOMAHAWK Launcher No. 7, an incident overpressure of 12.2 psi can be calculated for the launcher. This exceeds the design overpressure of 10 psi for the launcher. Therefore, the testing was considered finished at round 25. The reflected pressure measurements of P19 on the launcher show that the incident pressure was no more than 13.3 psi on round 25.

The reflected overpressure on the Fueling at Sea Outrigger was measured through round 23. The pressures from rounds 24 and 25 exceeded the range of the instrument (60 psi) and could not be recorded. The reflected overpressures in excess of 60 psi show that the incident pressure was at least 20 psi on the arm.

The incident overpressures were well below the equipment design values for Mount 23, the HARPOON launchers, and the Glide Slope Indicator.

V. Response Of Critical Equipment Items

A. CIWS Mount 21

It was originally planned to install a strain gauge rosette on the track radome of Mount 21. It was subsequently learned that reliable strain measurements could not be made on the radome material, and that the barbette panels of the weapon were of equal concern with respect to blast loading. Since the barbette panels are of sandwich construction with sheet aluminum on the outside layer, strain response could be easily and reliably measured. The instrument for strain measurement on Mount 21 was therefore shifted to the center of the barbette panel.

Prior to the test General Dynamics indicated that failure of the barbette panels occurs in static tests in the range of 2000 to 2500 microstrain in any arm of a rosette. The failure consists of delamination of the aluminum from the filler/spacer material between the aluminum sheets. The strains measured during the firings are plotted against the reflected overpressure measured very near the strain gauge. There is good correlation between the strain arm in the vertical direction and the measured reflected overpressure. The principal strain also correlates even better with the pressure. The strain values lie in the critical range as determined from static testing, although no failures are apparent. The values measured from round 13, however, are hard to explain. The strain from this round has not increased in accordance with the increase in pressure measured. Because the strains on Mount 21 were in the critical range, and damage occurred to the SLQ-32 on this same round, the test objectives had been met at round 13. The pressures measured at the P1 and P2 locations were 5.92 and 5.95 psi respectively. Because the overpressure decays rapidly with distance, these data indicate that the incident pressure at Mount 21 was very near the planned value of 5.0. The track radome reflected

CHAN.	LOCATION	19	20	21	22	23	24	25
P10	GSI, Incident	1.99	2.56	2.20	1.45	1.89	1.02	1.18
P11	ABL No. 7, Incident	5.30	6.65	6.74	10.61	10.97	12.04	15.19
P13	Harpoon, Incident	1.65	2.36	1.97	2.52	2.33	2.75	3.30
P14	Mount 23, Incident	1.30	1.92	1.59	1.73	2.70	1.87	2.77
P17	Ras Sta., Reflected	20.9	22.6	28.1	45.17	54.0	Sat.	Sat.
P19	ABL No. 7 Reflected	11.7	16.7	19.1	29.4	26.8	34.9	35.8
P20	MT 23, Reflected	6.1	5.49	6.00	7.12	2.89	3.05	3.25

TABLE 4

overpressure was 11.7 psi, which indicates the incident pressure at the radome was 5.1 psi, in agreement with the plan and the values measured at P1 and P2.

There were numerous circuit breaker failures during the firings. They were frequent, random and do not correlate with overpressure. Breakers No. 20 and 22 opened most frequently. No. 8 and No. 5 each opened twice. No. 28 opened once. They were not damaged and could readily be reset and the system brought back on line. The rubber boot connecting the electronics enclosure to the barbette pulled out of its frame. The heat exchanger in the magazine pulled away from its mounting stanchions, Figure 13. Leaks in the heat exchanger existing prior to the test were made worse and caused flooding of the magazine. The search radome rotates slightly as a result of gun blast. The radomes can rotate far enough for the latches to become ineffective. The radomes rotated approximately 1/16-inch during the test.

The mounts successfully completed preaction calibration (PAC) firings during and after the main battery firings.

In summary, the CIWS Mount 21 was systematically exposed to a number of blast loads in the range of 3.4 to 5 psi. The data indicated that the system survived these exposures and functioned reliably afterward, but operation was temporarily interrupted. The measured strain data correlated well with the pressure data. The strain data indicate that the system may be on the verge of failure at these blast levels. Because the strain response to the final round was not as large as would be predicted, the barbette panel should be carefully inspected by the manufacturer for possible concealed damage or impact on internal structures. Firings of Turret No. 3 had no apparent effect on Mount 23, other than an incident of circuit breaker tripping.

B. SLQ-32(V)3 Electronic Countermeasures Set

The SLQ-32(V)3 system aboard NEW JERSEY had experienced problems during previous main battery operations as previously discussed and explained in reference (12). Therefore, Mr. Edward E. George, a NSWC Electronics Engineer who specializes in the SLQ-32 system, was assigned to the test team. Upon arrival at the ship Mr. George was briefed on the status of NEW JERSEY's system and its deployment history. Mr. George performed system diagnostic tests to baseline the system. He found a need for correlation adjustments in band 3. He also noted a leveling problem in the portside antenna. He concluded that the existing faults would not seriously affect the planned testing.

The ships crew reported that the enclosure door latches would be destroyed unless the inspection plates were removed from each enclosure. They reported that the removal of the plate before main battery firings is a standard procedure. The technical argument for removal of the inspection plates seemed barely plausible to the test conductor. However, since removal of the inspection plates was a standard procedure, and leaving them in place would not prove anything one way or another, their removal for the test was authorized. The upper latch on the forward edge of the starboard, forward radome door, and both latches on the port, aft, transmit door broke as a result of round 4. The door had to be lashed down and the interlock had to be defeated to continue the test.

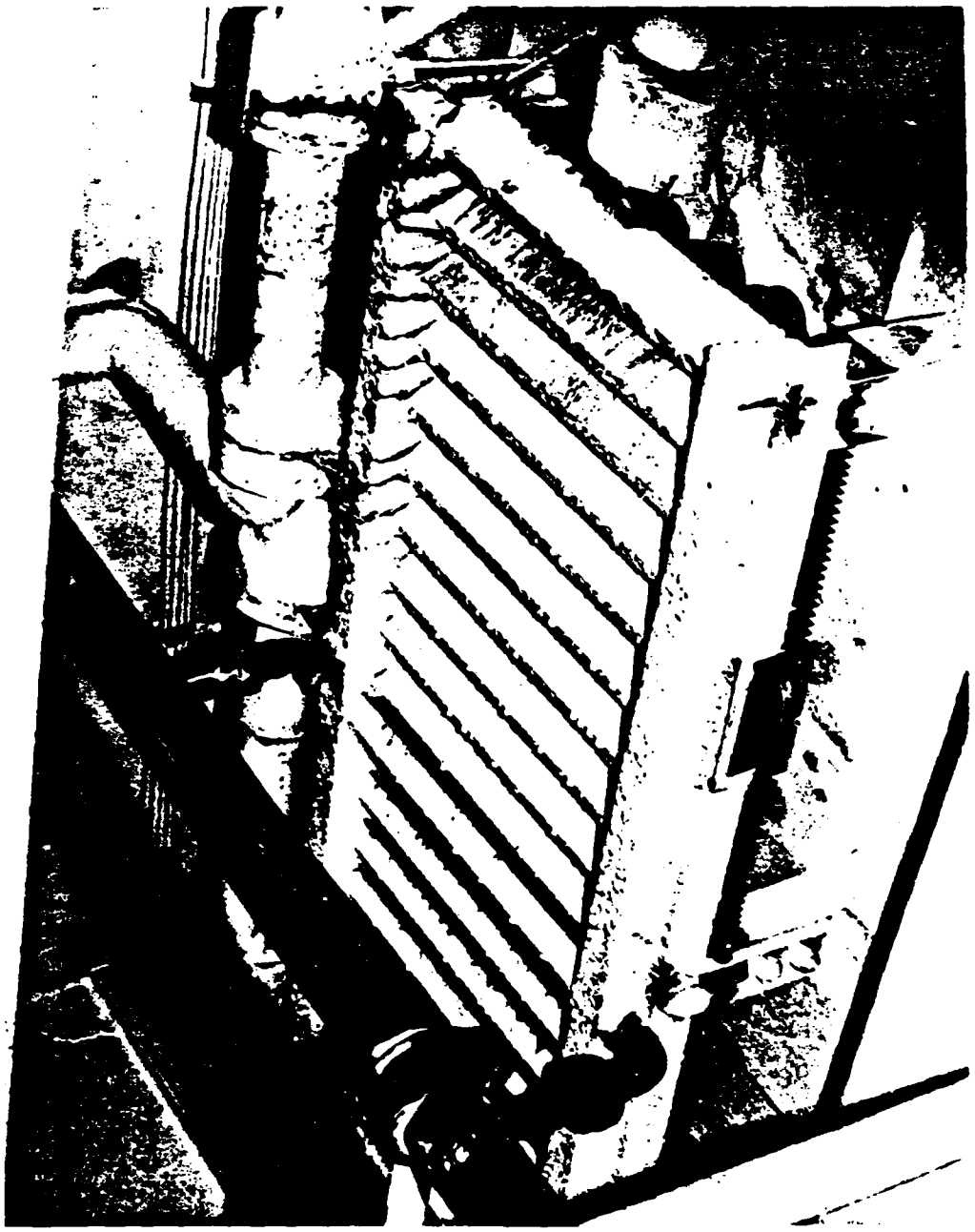


FIGURE 13. DAMAGED HEAT EXCHANGER IN CIWS MOUNT 21 MAGAZINE. BROKEN WELDS WHERE THE TANK IS ATTACHED TO THE MOUNTING BRACKETS CAUSED FLOODING OF THE MAGAZINE.

The SLQ-32(V)3 system was fully operational during the test. Signals simulating threat emitters were injected into the system. The simulated threats were being engaged by the system during the firings. The engagements consisted of combined transponder and repeater techniques. Numerous system faults occurred as a result of the firings at the instant of firing, but the system always restored itself to full operation until round 11, when high voltage power supply unit 3A10 went down permanently. The system gracefully degrades to a reduced power mode upon loss of a single high voltage power supply. On round 12 the starboard ECM dropped out and returned momentarily later as before. On round 13 the starboard high voltage was lost, the forward transmit radome was broken, and the top latch on the starboard forward radome door was broken. The radome was repaired with tape and the system functioned normally (at reduced power due to loss of high voltage power supply 3A10). The effect of a broken radome on radiated power and antenna directivity are unknown. The forward firings were completed at round 13. The system diagnostic tests were run again. Except for problems directly related to high voltage power supply 3A10, the system performance was essentially unchanged. A horizontal crack was found in the receive radome, Figure 14.

The system response to Turret III firings was essentially similar, with Electronic Countermeasures (ECM) drop outs at each firing. Problems were still experienced with interlock switches. For several of the Turret II firings, the battle short switch was closed. This effectively prevented ECM drop outs. Appendix B of this report contains a verbatim transcription of Mr. George's notes taken during the firings.

After the firings were completed, the countermeasures receiver R-2124/SLQ-32(V) and power supply PP-7504 ISLQ-32(V) were found loose in their racks. The AN/SLA-10B blanker was ready to break loose from the bulkhead.

After the ship arrived in Long Beach, Raytheon Service Company representative Mr. J. R. Lipman made a detailed inspection of the system. His trip report is reproduced as Appendix C of this report. With the exception of the last sentence of his paragraph 2.6.4, his report appears to be complete and correct. His conjecture in paragraph 4.2 that the latch failures occur during the negative overpressure phase after passage of the blast wave over the equipment has merit and should be pursued by analysis and pull tests of the latches.

An essential result of this test is that the same types of damage resulted in the starboard system as already existed in the port system due to firings from angles that complied with the existing adminstrative restrictions on relative train. Although the starboard damage was new, and the direct and obvious result of firing from larger angles than previously allowed, one could expect similar damage to occur again after a number of firings at a lower overpressure level.

Appendix D, from the test conductors notes, is a discussion of the strains measured in the forward outboard door rail of the portside antenna. The strains are plotted against reflected overpressure in Figure 12. The measured strain correlated well with the reflected overpressures measured on the antenna. Since the exact point on the outboard door rail where the strains are largest is

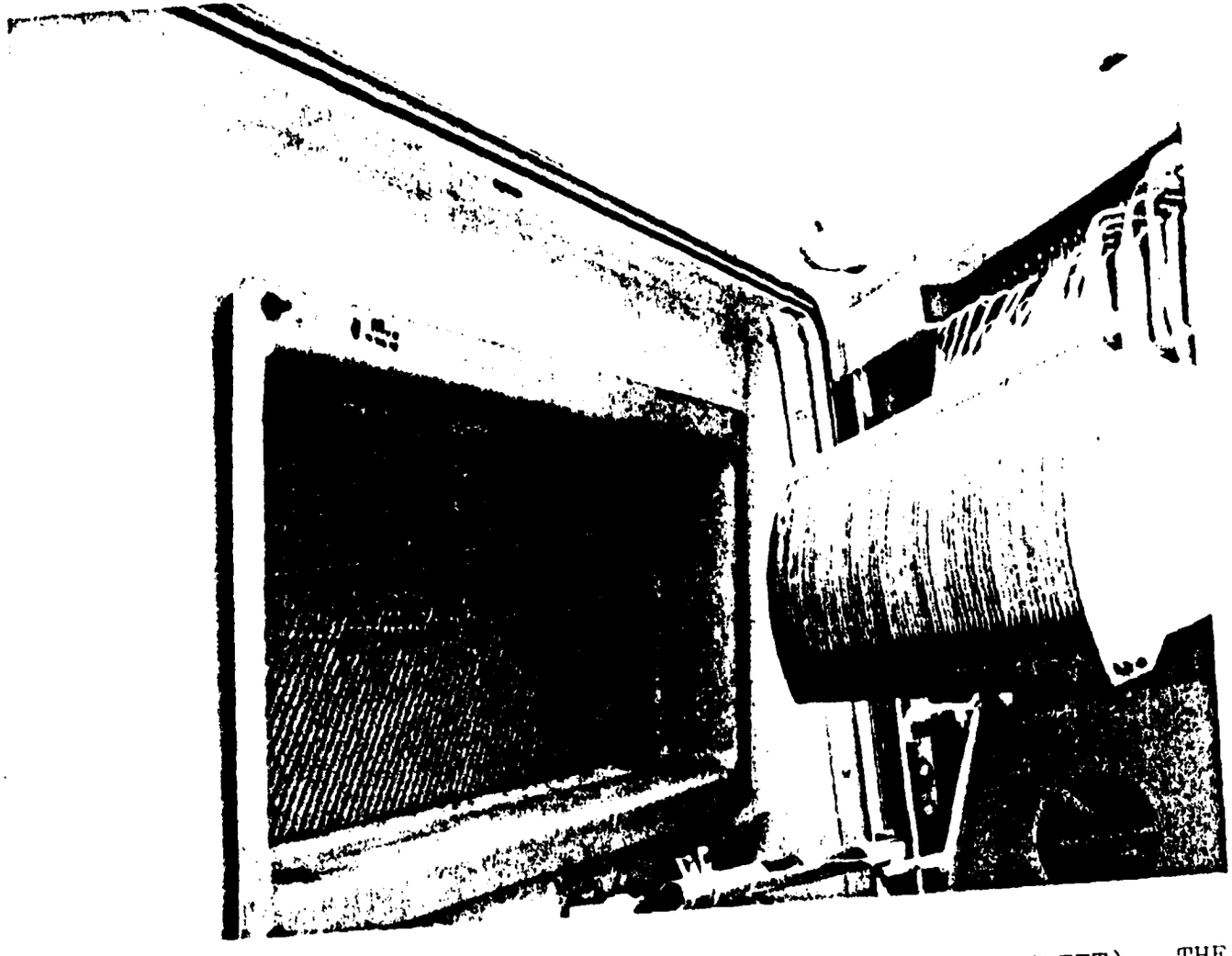


FIGURE 14. SLQ-32(V)3 RECEIVE ANTENNA (RIGHT) AND RADOME (LEFT). THE ENCLOSURE IS OPEN FOR INSPECTION. THE RADOME HAS A HORIZONTAL CRACK.

not known, it is unlikely that the instrument was at the point of maximum strain. The data show that stresses at these overpressures are quite large. Potentially serious structural failures could occur at even slightly higher overpressures.

The largest measured stress and strain were checked against the critical stress using all the common theories of failure, i.e., the maximum normal stress theory (Rankine), maximum shear theory (Coulomb), maximum strain theory (Saint-Venant), maximum distortion energy theory (Huber, vonMises, Hencky), and the maximum strain energy theory (Beltrami). The results were that the measured stress (strain) was 58%, 58%, 54%, 53%, and 55%, respectively, of yield. These calculations do not employ any safety factor, and are based on strains measured at some point other than the maximum. The endurance limit in fatigue of 6061-T6 aluminum is 14,000 psi (1400 microstrain), which is considerably under the stress of 21,480 psi actually measured on round 13. Therefore, the design is very marginal under the blast loads from Turret II.

C. TOMAHAWK Launcher

The decay in overpressure with distance near the gun is very rapid. At the 10 psi location corresponding to the left barrel firings of Turret III with respect to Armored Box Launcher (ABL) No. 7, the wave decays 1.5 psi in 4 feet of travel (90° radial). The measurements of pressure for the left barrel at P11 in the range of 10 psi (rounds 23, 23, and 24) must therefore be reduced 1.5 psi to obtain the incident pressure on ABL No. 7. The incident pressures from rounds 22, 23, and 24 are therefore, 9.1, 9.5, and 10.5, respectively. The overpressure at P11 for round 25 measured 15.19 psi; it must be similarly reduced 3.0 psi to account for the decay in traveling from the instrument to ABL No. 7. The estimated incident pressure is therefore, 12.2 for round No. 25. Since this overpressure exceeded the ABL design criterion of 10 psi, the test conductor recommended terminating the test. Rounds 26 and 27 were not fired. The reflected overpressure measured by P19 agrees with expected values based on the incident values measured by P11.

The only damage observed was a 3-inch crack in the armor skirt attached to the top half of the box to protect the interface between the top and bottom sections when the launcher is stowed. It is not certain that this damage is new, and may have been concealed by paint which was torn away by the blast. The damage was insignificant. The launcher functioned normally after the firings. No discrepancies were found in any of the launcher equipment.

D. HARPOON Launchers No. 1 and 3

The highest incident overpressure at HARPOON Launcher No. 3 was 3.3 psi, this is well under the 7 psi design limit for the launcher. The aft closure of the forward, lower cell of Launcher No. 1 was torn by the blast. The blast wave reaches a large vertical bulkhead below Mount 23 soon after passing over the HARPOON canisters. The reflection off the bulkhead then provides a second load on the canister covers that may increase the pressure above the measured 3.3 psi incident value.

E. Glide Slope Indicator (GSI)

The highest overpressure measured at the Glide Slope Indicator (GSI) was 2.56 psi. The instrument and GSI are as shown in Figure 15. Upon arrival at the ship it was learned that the GSI head is normally removed and stowed for main battery firings in NEW JERSEY. The instrument that had been originally planned for measurement of the reflected overpressure at the GSI fresnel lens was therefore made available for another location. Because no problems were expected with the GSI, the system was not inspected for possible damage existing prior to the test. After the firings the GSI had damaged helicoils in the stabilized platform where the hydraulic actuator rods attach to the platform. These were repaired by the ship. There was a problem in stabilizing the platform in certain modes of operation after the platform was repaired. The fault had not been isolated by the time the test team departed the ship. The ship subsequently reported damaged welds in the transformer enclosure, reference (14) The forward platform securing stanchion was found almost broken off at its root. The stanchion design is inadequate. The GSI was extensively tested at 7.0 psi from a 5"/54 caliber gun at Dahlgren in 1976, reference (13), with the head in place and the system operating in a normal mode. Additional information is presented in reference (15).

F. Fueling At Sea Outrigger

The instrument not needed for the measurement of the GSI fresnel lens reflected overpressure was installed on the Fueling at Sea Outrigger. The instrument was approximately one half way up the outrigger arm, approximately one foot below the top surface, installed facing aft on the vertical surface. The measured reflected overpressure for round 23 was 54 psi. The measurements for rounds 24 and 25 exceeded 60 psi and saturated the recording equipment. The incident overpressures were probably around 20 psi. The two outermost stanchions forward and three outermost stanchions aft were pulled from their foundations by blast from rounds 24 and 25. The service platform was deformed. The hoses had been lowered and were not damaged. Lighting equipment installed on the outrigger was damaged. The handrail for the ladder was torn loose.

G. SPS-49 Search Radar

The SPS-49 radar would not radiate after round 3. The klystron was replaced and the system radiated and the antenna rotated, but a problem remained in elevation stabilization of the beam. The beam elevation problem was not repaired at the time the test team left the ship.

H. AN/SSR-1 Satellite Communications Antenna

The portside satellite antenna was broken by round 12. The starboard unit, which is identical and symmetrically located, was not damaged. Evidently, the portside antenna had been damaged in previous operations and was on the verge of failure. The portside antenna is protected from blast during firings to starboard by the bridge spray shield. Weak gun blast or structural borne vibration of the antenna foundation caused catastrophic failure of the circular elements of the antenna.

FIGURE 15. STABILIZED GLIDE SLOPE INDICATOR (GSI) AND SPONSON. TURRET III SHOWN IN BACKGROUND. INSTRUMENT P10 FOR MEASUREMENT OF INCIDENT OVERPRESSURE AT GSI SHOWN POINTING IN APPROXIMATE DIRECTION OF GUN MUZZLES DURING TEST. SEVERAL INTERNAL STRUCTURES WERE FOUND DAMAGED AFTER TURRET III FIRINGS.

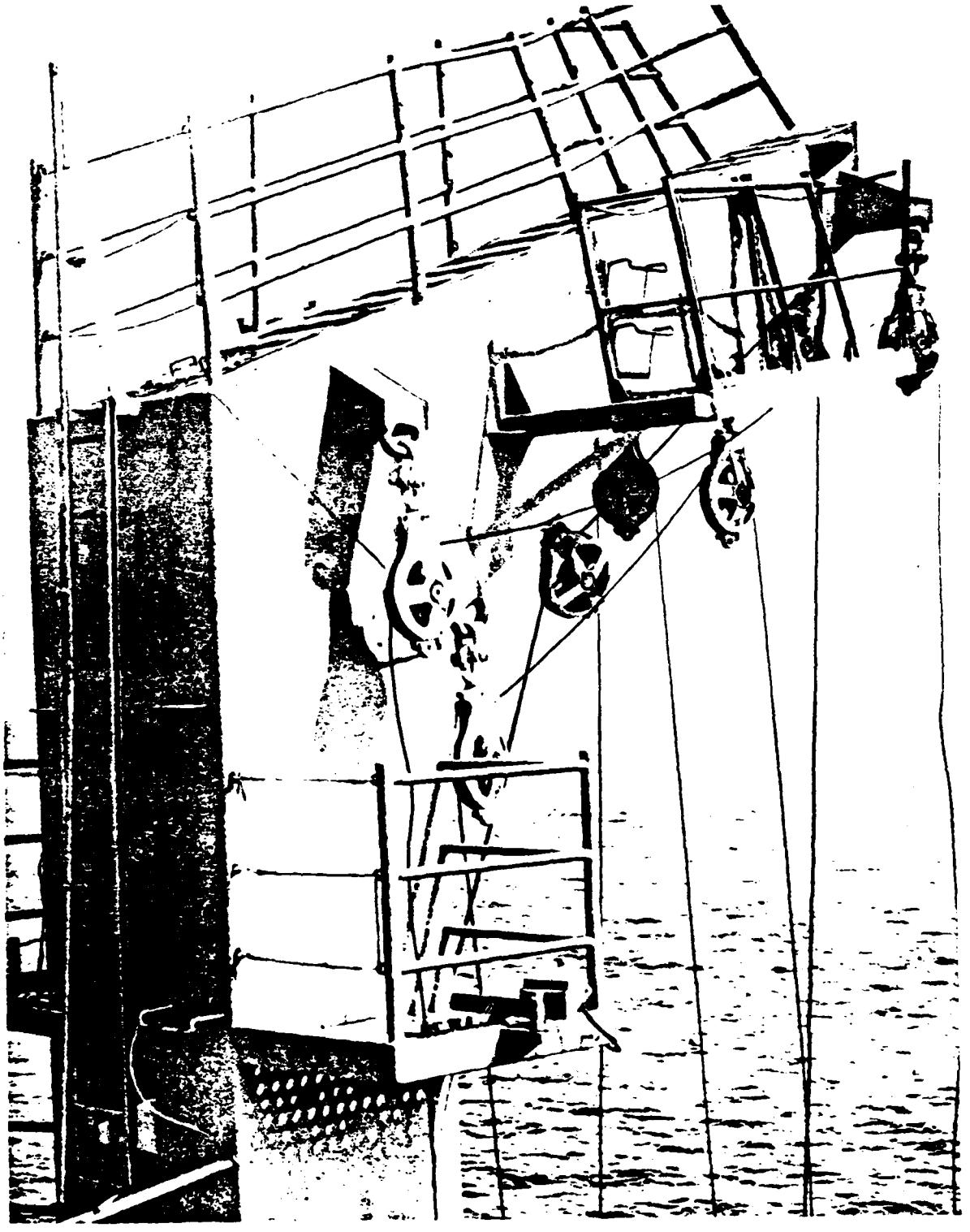


FIGURE 16. FUELING AT SEA OUTRIGGER. LADDER HAND-RAIL, RAILINGS ON ARM, AND SERVICE PLATFORM WERE DAMAGED BY BLAST FROM TURRET III. P17 MEASURED REFLECTED OVERPRESSURES FROM THE LEFT BARREL OF TURRET III IN EXCESS OF 60 PSI.

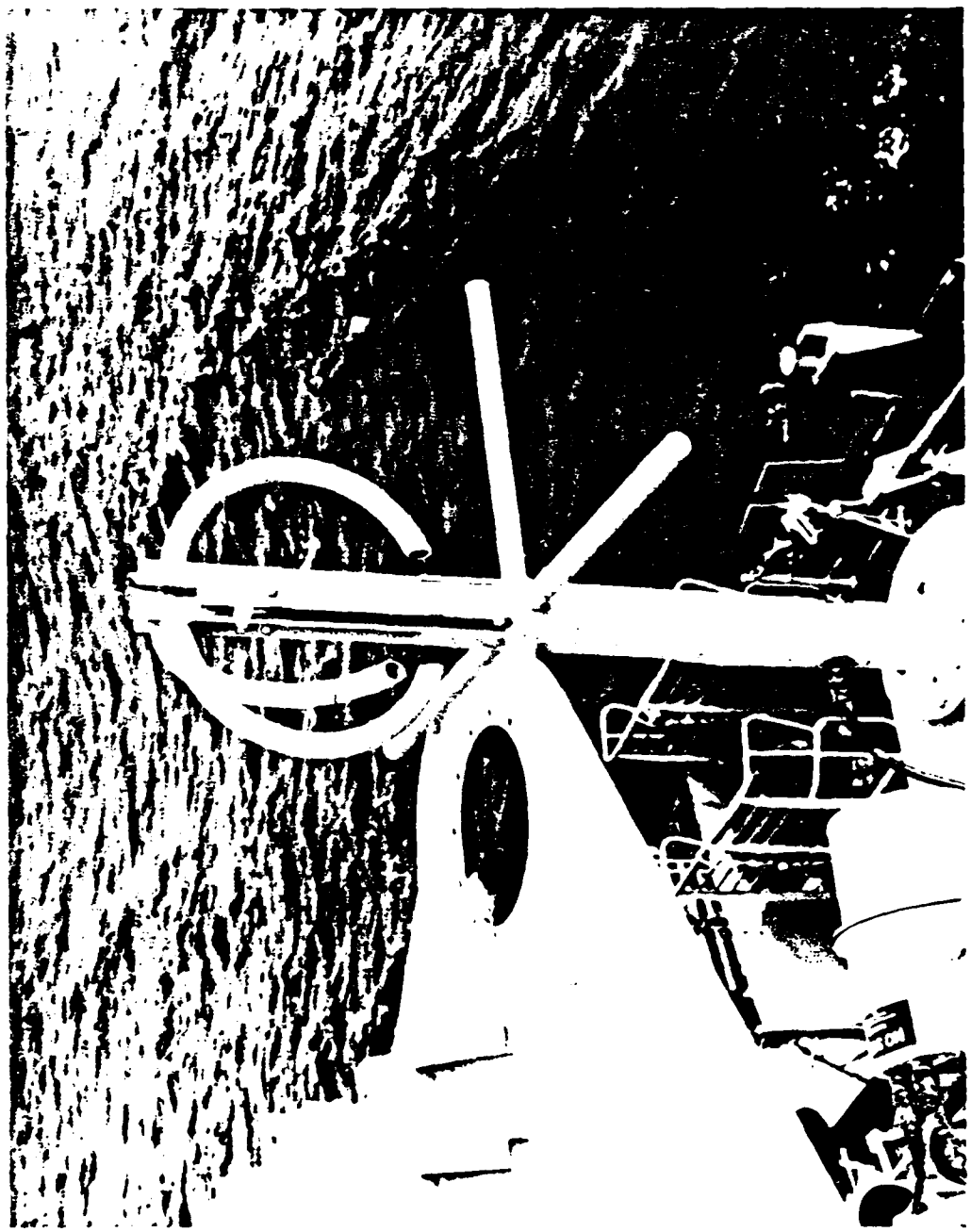


FIGURE 17. AN/SSR-1 SATELLITE COMMUNICATIONS ANTENNA, FORWARD, PORTSIDE UNIT. PHOTOGRAPH SHOWS ONE SEMICIRCULAR ELEMENT MISSING, ANOTHER BENT AND MISALIGNED AS A RESULT OF TURRET II FIRINGS. DAMAGE IS REMARKABLE IN THAT ALL GUN FIRING WAS TO STARBOARD.

I. Additional Damage Reported By Ship

A. Reference (10) reported several additional items of damage which are summarized below:

1. 04 level bridge wing. Three vertical gussets for the starboard spray shield had cracked welds at the intersection of the gusset with the deck. There was old damage concealed by paint. These welds had obviously been repaired by adding weld numerous times. They can be patched again, or the old material can be ground away to make room for a larger reinforcement. The starboard rudder angle indicator housing was broken off from its mounting bracket. The failure of the mounting showed rust in old cracks that were concealed by paint prior to the test. The mounting should be repaired by grinding away old material and welding, or providing a new bracket.

2. Captain's Gig and Motor Whale Boat. There was a narrow vertical crack in the aft cabin door from top to bottom and a communications antenna was broken on the Captain's Gig. A fuel tank in the Motor Whale Boat was ruptured. Both boats are starboard. There simply isn't any good place to store the boats on the modernized battleships and nuisance damage will continue unless they are relocated or launched prior to firing.

3. Gyro Repeater on 08 Level Bridge. The centerline gyro repeater glass was broken. The gimbal pins sheared in the starboard side gyro repeater. These items should be repaired and adequate spare parts should be carried for future repairs.

4. Speakers. Numerous speakers were damaged by the firings. A total of ten 1MC speakers were put out of commission: two on the 05 level forward, one on the 08 level bridge, five on the main deck forward, one on the main deck aft, one on the fantail. Four 5MC speakers were damaged: two on the main deck aft, portside, one on the main deck forward, starboard side, and one on the fantail. 18MC speakers were damaged on the 04 level bridge and the 08 level bridge. The locations of the speakers should be reviewed for possible relocation to areas with better protection. Protective covers could be provided for use when setting zebra or firing 16-inch guns.

5. Lights. The starboard running light and lights on the Fueling at Sea Outrigger were damaged. Damage to lights is frequent during gun firing. Adequate spares must be carried.

VI. Recommendations

A. Navigation and Tactical Employment of Main Battery

The combined results of the Phase II structural test firings, reference (5), and the present firings provide a clear understanding of the capabilities and limitations of the main battery with respect to arcs of fire. Administrative restrictions were placed on the firing arcs of Turrets II and III as a result of the Phase II tests, but the effects of exceeding these limits could not be predicted. Very specific recommendations can now be made, and the effects of exceeding the previously recommended limits are known. The present results bear directly on planning Naval gun fire support, target selection, sequence of target engagements, and navigation.

Turret I remains unrestricted and can be fired from any position in the sector allowed by the positive stops in the turret. Turrets II and III should be restricted to prevent blast damage to equipment. It is possible to describe the firing zone of Turrets II and III in terms of a "routine engagement sector," a "caution zone," and a "danger zone."

Turret II should continue to abide by the recommendations of reference (5) for routine engagements. These limit the left barrel to 125°30' relative, center barrel to 120° relative, and the right barrel to 114° relative. The enlarged firing sector explored in this test can be used with caution. However, the ship can expect self-inflicted damage that may cause temporary loss of capability for other types of warfare as a result of such firing. It should be the tactical decision of the Commanding Officer to fire from the "caution zone." It is easy to visualize situations where the risks of firing in the caution zone are acceptable. The caution zone for the left barrel is 125°-30' to 138° relative; the center barrel is 120° to 134°-20' relative; and the right barrel is 114° to 124° relative. The caution zone for the center and right barrels of Turret II begins forward of 46° relative train and extends forward to 42° relative. The caution zone for the left barrel is 51° to 46° relative. Firing from the caution zone causes blast loads on TOMAHAWK Launcher No. 7 to exceed design limits. Although this did not damage the launcher significantly, it could damage missiles stowed in the launcher. The zones are shown in Figures 18 and 19.

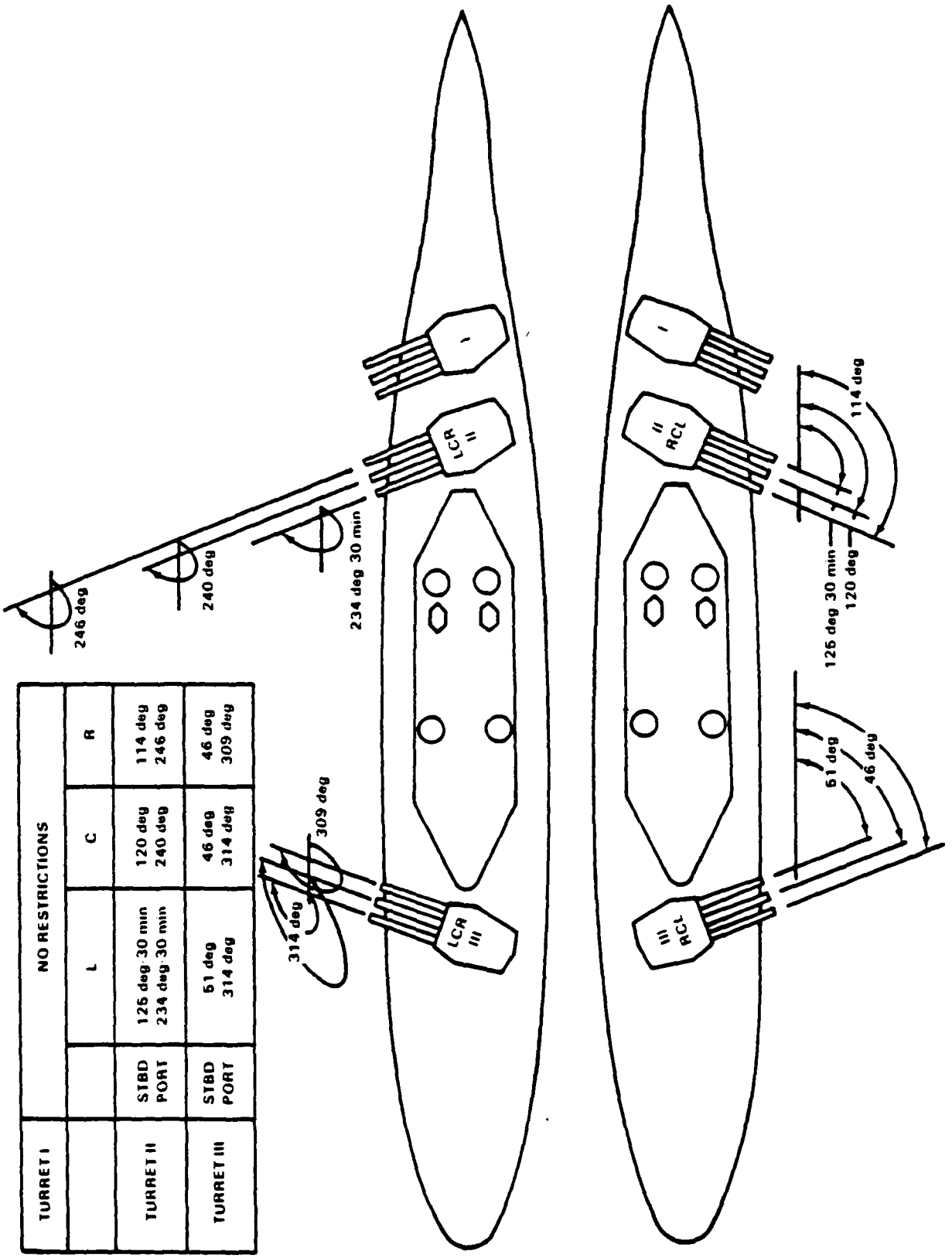
The routine engagement zones and caution zones are symmetrical about the centerline of the ship. The portside zones are also shown on the figures.

The "danger zone" for Turret II begins at 138° relative for the left barrel, at 134°-20' relative for the center barrel, and 124° relative for the right barrel. Firing Turret II from trains abaft of these values will probably cause serious structural damage to the forward CIWS mounts and the SLQ-32 Electronic Countermeasures Set. The strain instrumentation results from the present tests clearly show there is no margin of safety when firing from the edge of the caution zone. Firing forward of the caution zone from Turret III could cause a projectile to strike refueling at sea equipment or cause unpredictable blast damage to the TOMAHAWK and HARPOON missiles and launching equipment. There have been no firings from a modernized battleship from positions inside the danger zone. Other equally serious, but unforseeable, damage may result. It would be a most serious tactical decision to fire from the danger zone.

B. Equipment Recommendations

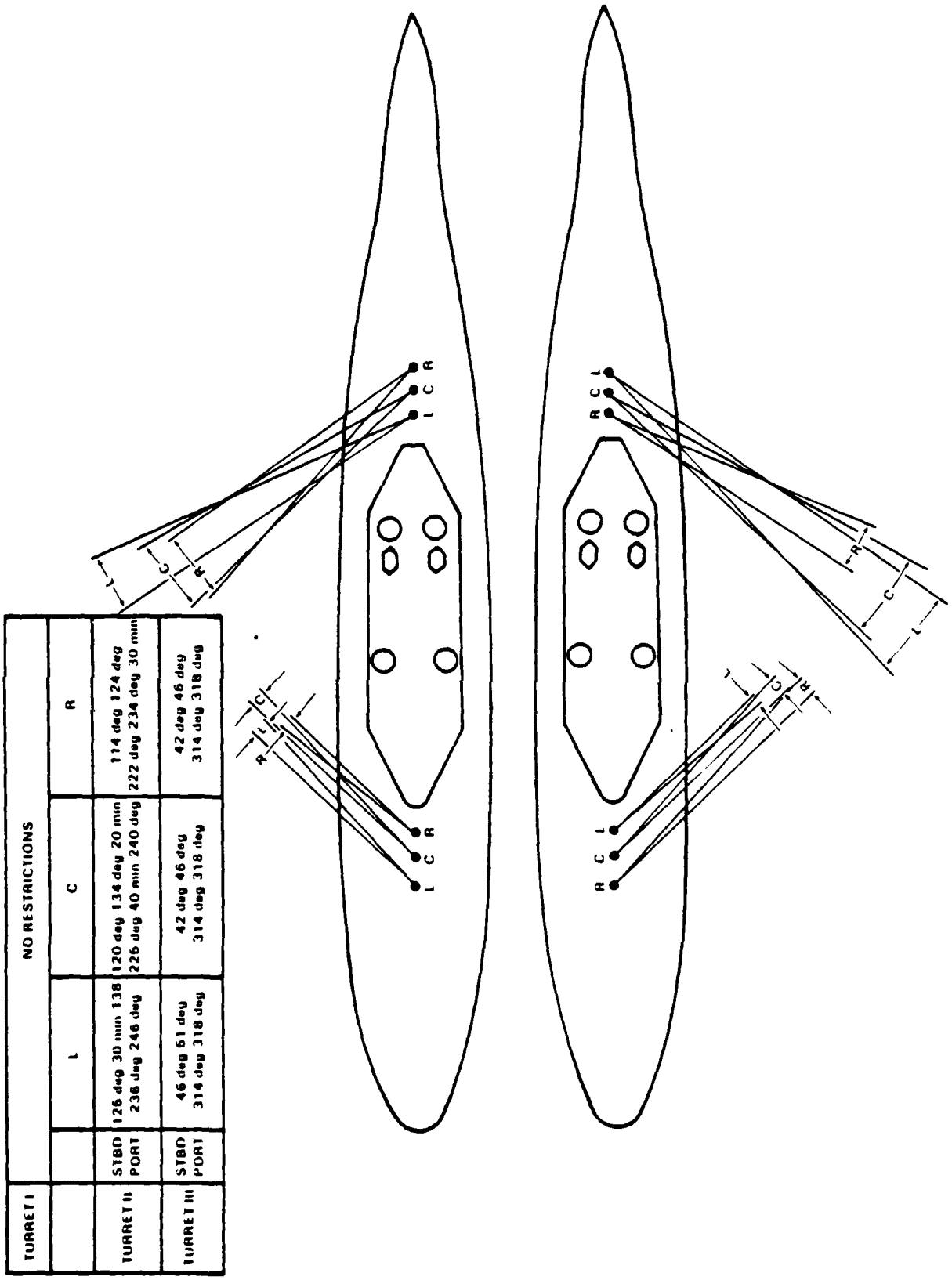
1. PHALANX Close-in-Weapons System.

The most serious fault with the PHALANX System was inadvertent tripping of circuit breakers. This is believed to be a generic fault with the system rather than a fault peculiar to Mount 21. The high level of experience and training of the NEW JERSEY CIWS personnel enabled them to respond quickly to the faults and reactivate the system. The system is required, however, to operate continuously. Improved breakers or better mounting of the breakers is therefore required.



TURRET I	NO RESTRICTIONS			
		L	C	R
TURRET II	STBD PORT	126 deg 30 min 234 deg 30 min	120 deg 240 deg	114 deg 246 deg
TURRET III	STBD PORT	51 deg 314 deg	46 deg 314 deg	46 deg 309 deg

FIGURE 18. ROUTINE ENGAGEMENT ZONE



TURRET I	NO RESTRICTIONS			
		L	C	R
TURRET II	STBD	126 deg 30 min 138 deg 236 deg 246 deg	120 deg 134 deg 20 min 226 deg 40 min 240 deg	114 deg 124 deg 222 deg 234 deg 30 min
	PORT			
TURRET III	STBD	46 deg 61 deg 314 deg 318 deg	42 deg 46 deg 314 deg 318 deg	42 deg 46 deg 314 deg 318 deg
	PORT			

FIGURE 12. CAUTION ZONE

Blast causes the search radomes on Mounts 21 and 22 to rotate. This rotation would not be significant for just one blast event as for nuclear blast or warhead blast, but is significant on the battleship. The track radome from Mount 22 was blown off on two occasions in previous operations. The rotation problem should be fixed by keying the interface or modifying the latches.

Numerous stress cracks were observed on the Mount 21 track radome prior to the test. These are concentrated around the mounting screws. Each crack and its extent were noted prior to the test. The cracks were not enlarged by the firing, and therefore, do not appear to be related to gun blast. Similar cracks were not observed on Mount 22. The cause of the cracks should be determined.

Strains in the range of static failure of the barbette panel were measured at the 5 psi incident overpressure level. Since gun blast loads are of relatively short duration as compared to warhead or nuclear blast, 5 psi can be taken as an upper limit for survivability under various forms of attack. An improvement in the barbette panel design could lead to improved survivability and enlarged firing zones for the battleships. The cause of the anomalous strain reading of round 13 should be investigated.

2. SLQ-32(V)3 Electronic Countermeasures Set.

It is the opinion of the test conductor that the internal design of the SLQ-32 antenna from the mechanical standpoint is very good and will be adequate for any gun blast situation on the battleship. However, the enclosures, latches, and radomes need further development. The framework supporting the enclosure needs to be strengthened. Stronger structural elements, bolting and welding rather than riveting, and intermediate support for long members and large panels are recommended. The enclosures and radomes should not be allowed to impact the antennas, but should be supported by the antennas or other structures during blast loading.

The cause of failure of power supply 3A10 should be determined. Mr. Lipman's observations with regard to the shock mounting of inside equipment should be taken for action. The AN/SLA-10B Blanker should be relocated or shock mounted. The significance of momentary interruption of ECM as a result of gun fire should be assessed. If the fault is serious, its cause should be isolated and corrected. These faults occurred even during the relatively low overpressure blasts from Turret III. The battle short switch is not a viable remedy because it requires communication and a countdown for each shot, and the protection of bypassed interlocks and circuit breakers is lost. It was employed during the test only for diagnosis of the problem. Investigation of the problem does not require firing from the "caution zone" and can be carried out during routine training or practice firings.

3. TOMAHAWK Launchers.

a. Armored Box Launcher

The incident overpressure on TOMAHAWK Launcher No. 7 exceeded the design specification value of 10 psi. However, the design specification is not specific as to the wave form, angle of approach, or effect of nearby structures. Gun blast waves are of short duration and short length (on the order of 10 feet long). A 10 psi gun blast wave from Turret III does not pressurize the entire launcher to 10 psi at anytime as would a 10 psi wave from a nuclear explosion (at least 300 feet long). The short duration 10 psi waves from Turret III should be easily tolerated by the launcher. It may be possible to show that even higher gun blast overpressures are acceptable. Techniques are available for analyzing the gun blast interaction with the launcher, and comparing the loads with the design requirements. Such an analysis would be worthwhile and bear directly on an assessment the internal environment for missiles inside the launcher.

b. TOMAHAWK Missiles.

The gun blast induced vibration and acoustic environment inside the TOMAHAWK launchers is a concern. The acoustic field was measured to be 186 dB during the Phase II firings of reference (5). The incident overpressure was 6.95 psi. No attempt was made at measuring the acoustic field during the present tests. Significant vibrations, which have not yet been measured, may also be present. A preliminary assessment of the acoustic and vibration issue should be carried out. This may result in a requirement for further measurements at sea, or special restrictions on the train of Turret III when the after launchers are loaded with TOMAHAWK missiles.

4. HARPOON Missiles and Launchers.

The only discrepancy in the HARPOON equipment was a torn aft canister closure of the lower forward cell of Launcher No. 1. This is the point of highest overpressure due to reflections from the superstructure and deck of the ship. The failure was not serious and was readily repaired with a spare closure. No further action is required.

5. Stabilized Glide Slope Indicator

The glide slope indicator was found visibly damaged after the test was completed. Helicoil threads for the stabilized platform were stripped and the forward securing stanchion was broken at its root. This is surprising in view of the thorough testing done at the Dahlgren Laboratory in August 1977, reference 13. The tests at the Dahlgren Laboratory subjected the glide slope indicator to 60 rounds of blast from a 5"/54 caliber Naval gun. The GSI was exposed in both operating and secured modes. Several positions and angles of incidence were provided. The first 20 rounds were at a nominal incident overpressure of 2.0 psi. Actual measurements of the incident overpressure were in the range of 2.0 to 3.1 psi. Then 6 rounds were fired at the 4.5 psi overpressure level, with face-on and side-on exposures. Actual measurements of the incident overpressure were in the range 4.8 to 8.4 psi. Then 30 rounds were

fired at a nominal incident overpressure of 7 psi in both operating and stowed modes and face-on and side-on orientations. The fresnel lens was fractured on the fourth round at 7 psi. An aluminum plate was taped over the lens to protect it from further damage, and the unit was exposed to the remaining rounds without incident. The lamp and platform operated during and after the tests with no apparent problems. The actual incident overpressures were in the range 6.7 to 8.6 psi. The duration of positive overpressure was 3 to 4 msecs in all cases.

NEW JERSEY removes the lamp and lens assembly from the stabilization platform in preparation for main battery firings. This is done to avoid cracking the fresnel lens. This and the foundation are the only significant difference between the NEW JERSEY installation and the test conducted at Dahlgren. The overpressures on NEW JERSEY were in the range of 1.02 to 2.56 psi and 3 to 4 msecs duration. The overpressures were in the same range during the Phase II firings of reference (5). Acceleration measurements were made in the Dahlgren tests. Because no problems were expected in NEW JERSEY, accelerations were not measured. It is possible that shock from the foundation is the problem rather than blast on the exposed components.

It is recommended that the existing GSI be repaired. A cover for the lense should be provided and used when firing Turret III to starboard, rather than removing the head. If problems persist, the acceleration of the foundation should be measured. The acceleration data could then be used to provide an improved foundation, rather than relocating the entire system.

6. Turret III.

There is a problem that prevents Turret III from training forward of 55°-48' when in automatic control from forward plot. This problem should be resolved so that the full firing zone of the ship is available.

7. AN/SSR-1 Satellite Communications Antenna.

One would have expected the starboard, rather than the portside, antenna to fail first. Under the present test conditions, the portside antenna was well protected by the bridge superstructure and spray shield. The antenna may have been seriously damaged mechanically, but not electrically, during previous operations. Vibration induced in the ship structure by blast may have caused the failure. Adequate spares should be carried until more information is available.

VI. References

1. NAVSEAINST 9110.1 of 14 Feb 1980

2. NSWC ltr N43:JJY:plt 8800/BB-62-1 of Oct 1982

3. NSWC ltr N43:JJY:plt 8800/BB-62-2 of Nov 1982

4. NSWC ltr N43:JJY:plt 8800/BB-62-3 of Feb 1983

5. NSWC ltr N43:JJY:ph 8800/BB-62-4 of May 1983

6. NSWC ltr N43:JJY:wjr 8800/BB-61-2 of Feb 1984

7. PCO IOWA Unclassified msg 161600Z of Feb 84

8. SEA 61WZ Point Paper of 12 April 1984

9. NSWC Unclassified msg 232040Z of Apr 84

10. USS NEW JERSEY Confidential msg 032105Z of May 84

11. Contract Specification for Countermeasures Set AN/SLQ/(V)3, ELEX-C-2410 of 31 Aug 79

12. AN/SLQ-32(V) Newsletter Comment Sheet, 6 March 1984, originated by OI Division, USS NEW JERSEY

13. Miller, R. E., "5"/54 Muzzle Blast Test and Mark 56 Missile Blast Calculations of a Stabilized Glide-Slope Indicator," NSWC/DL TR-3606 July 1977. Naval Surface Weapons Center, Dahlgren, Virginia

14. USS NEW JERSEY Confidential msg 042225Z of June 84

15. Naval Air Systems Command Confidential ltr 13830 ser 5511B3/104 of 15 June 1984 "Condition of the Stabilized Glide Slope Indicator Aboard USS NEW JERSEY (BB-62)"

RTTUZYUW RUEBJLA5373 1142357-UUUU--RUCKSUU.
ZNR UUUUU
R 232043Z APR 84
FM NAVSWC DAHLGREN VA
TO USS NEW JERSEY
INFO COMNAVSEASYSCOM WASHINGTON DC
COMNAVELEXSYSCOM WASHINGTON DC
PCO IOWA
NAVELEXCEN PORTSMOUTH VA
BT
UNCLAS //N02300//
SUBJ: MAIN BATTERY FIRING IN NEW JERSEY
A. USS NEW JERSEY 191638Z APR 84
B. COMNAVSEASYSCOM WASHINGTON DC 181320Z APR 84
C. NSWC LTR E53:JJY:WJR 8800.4 OF APR 5 84
D. NSWC LTR E53:JJY:WJR 8800/BB-81-2 OF FEB 1 84
1. DATA REQUESTED BY REF (A) TO CONDUCT TESTS OF REF (B) PROVIDED BELOW. REF (C) STATED THAT THE TESTING REQUIRED TO ENLARGE MAIN BATTERY FIRING ARCS OF IOWA CLASS COULD BE CARRIED OUT IN EITHER IOWA OR NEW JERSEY. REF (D) WAS THE PLAN TO CARRY OUT THE TESTS IN CONJUNCTION WITH STRUCTURAL TEST FIRINGS (STF) IN IOWA. TIME CONSTRAINTS DUE TO ACCELERATED PRODUCTION SCHED FORCED COMPROMISES IN PLAN TO REDUCE IT TO ONE DAY FOR BOTH ROUTINE STF AND FIRING ARC ENLARGEMENT TESTS. ROUTINE STF NOT REQUIRED ON NEW JERSEY AND 27 ROUNDS NOW ALLOCATED FOR FIRING ARC ENLARGEMENT. TEST PLAN IS REF (D) MODIFIED AS FOLLOWS: CANCEL ALL HARPOON/5"/ RBOC/CIWS STF. REVISE TABLE 1:

ROUND	TURRET	BBL	TRAIN DEG	EL DEG	EXPECTED OVERPRESSURE. MT 21 PSI	SLS-32 PSI
1	2	L	123	45$	3.5	3.2
2	2	R	117	45	3.8	3.5
3	2	L	130.5	45	3.7	3.6
4	2	R	120	45	4.3	3.8
5	2	L	132.5	45	4.0	4.0
6	2	R	122.5	45	4.6	4.1
7	2	L	134	45	4.1	4.3
8	2	R	122.5	35.5	5.	3.8
9	2	L	134.5	45	4.2	4.6
10	2	R	123	39	5.	4.0
11	2	L	135.5	37.5	4.5	4.6
12	2	R	124	44	5.	4.6
13	2	L	138	30	5.	4.6

DRAFTED AND RELEASED
BY NAVSWC: E53
INFO: C, E

ROUND	TURRET	BBL	TRAIN	EL	EXPECTED OVERPRESSURE MT 21	SLQ-32
14S	2	R				
15	2	L				
16	2	R				
17	2	L				
18	2	R			MT 23	THWK NO.7
19	3	R	51	30	2.3	4.
20	3	R	46S	30	2.4	4.7
21	3	C	51	30	2.6	5.
22	3	C	46	30	2.8	5.8.8
23	3	L	51	30	2.9	6.
24	3	L	46	30	3.2	7.2
25	3	L	46	25	3.2	7.6
26	3	L	46	22	3.1	7.8
27	3	L	46	18	3.	8.

SRNDS WITH ELEVATION 45 DEG ARE TO BE FIRED FROM UPPER LIMIT; RNDS WITH RELATIVE TRAIN 46 DEG ARE TO BE FIRED FROM FORWARD LIMIT. RNDS 14 THRU 18 ARE DISCRETIONARY AND HELD IN RESERVE.

2. DESIGN GUIDANCE TO ORIG. FOR DESIGN OF SUBJ. TEST IS TO NOT EXCEED 5PSI ON CIWS RADOMES AND 4.5PSI ON SLQ-32. TESTING MUST STOP AT FIRST INDICATION OF DAMAGE TO EITHER.

3. THE APPROACH IS TO FIRE SINGLE ROUNDS AT INCREMENTALLY LARGER TRAINS GRADUALLY APPROACHING ABOVE LIMITS. SYSTEM TESTS, VISUAL INSPECTIONS, AND BLAST DATA TO BE ANALYZED FOR 20 MINUTES BETWEEN ROUNDS. TWO HOURS REQUIRED FOR THOROUGH SDT OF SLQ-32 AFTER ROUND 9. 24 HRS REQUIRED AFTER TURRET 2 TO MOVE TEST EQUIP. AFT FOR TURRET 3. RND 14 THRU 18 MAY BE FIRED FROM LARGER ARCS IF TEST LIMITS NOT ATTAINED AT RND 13.

4. MT 21 TO FIRE PACS BEFORE TESTS AND AFTER RNDS 8AND .3. MT 23 TO FIRE PACS BEFORE RND 19 AND AFTER RNDS 24 AND 27.

. SUGGEST RELOCATING GIG AND RAS HOSES FOR TEST.

6. TWO WORKING DAYS AFTER EMBARK REQD TO INSTALL EQUIPMENT. FWD CIWS WORKSHOP AND TOMAHAWK SERVICE ROOM NO.1 ARE REQUESTED FOR SETTING UP RECORDING EQUIPMENT.

7. SIX NSWC REPS TO CONDUCT TEST AND OPERATE EQUIPMENT UNDER SUPERVISION OF DR. JON J. YAGLA, MECHANICAL ENGR. GM14.

8. SPECIAL SUPPLEMENTARY PLAN FOR SLQ-32:

A. PRIOR TO EACH DAY OF FIRING RUN COMPLETE SDI. NOTE ANY FAULTS.

B. ALLOW SUFFICIENT TIME FOR HIGH VOLTAGE POWER SUPPLY STABILIZATION PRIOR TO FIRING.

C. INJECT AN EMITTER IN EACH SIDE, INSERT AN ONLINE LIBRARY ENTRY FOR EACH, AND ENGAGE WITH A COMBINED (TRANSPONDER AND REPEATER) TECHNIQUE.

D. DURING TEST MONITOR THE DCC FOR FAULTS AND ALERTS, AND OBSERVE OSCILLOSCOPE CONNECTED TO BOTH DETECTED TECHNIQUE VIDEO JACKS, 2A4J12 AND 2A4J13. NOTE ALL SYSTEM FAULTS, ALERTS, AND ECM TRANSMISSION TROUBLES.

E. CONDUCT VISUAL INSPECTION OF OUTSIDE ELEMENTS BETWEEN ROUNDS.

F. RERUN SDI IF SYSTEM FAULTS OCCUR, DURING LONG BREAKS IN TESTING, AND AT COMPLETION OF TESTING.

G. NSWC ENGINEER E. GEORGE ADDED TO CRIG TEST TEAM TO ASSIST WITH EW TESTS. NSWC TO FURNISH SCOPE AND SIGNAL GEN.

9. INSTRUMENTATION PLAN AS FOLLOWS: TABLE 9

CHAN	TUR	PURPOSE	LOCATION
P1	2	INCIDENT PRES. ON MT21	RAILING ON SPONSON FWD OF CIWS
P2	2	INCIDENT PRES. ON MT21	RAILING ON SPONSON FWD OF CIWS
P4	2	INCIDENT PRES. ON SLQ-32	RAILING FWD OF SLQ-32 13.4' STBD OF CL.
P5	2	REFLECTED PRES. ON SLQ-32	SURFACE MTD ON ANT. ENCL. 5'6" OFF DECK
P6	2	REFLECTED PRES. ON MT21 RADOME	SURFACE MTD ON TRACK RADOME AT 019DEG REL TO SHIP IN STOWED POS. 12'-0" OFF DECK
P7	2	REFLECTED PRES. ON MT21 ELEX ENCL.	SURF MTD ON ELEX ENCL PANEL
P8	2	REFLECTED PRES. ON M21 BARBETTE PANEL	SURF MTD ON BARBETTE PANEL

P10	3	INCIDENT PRES ON GSI	RAILING STBD OF GSI
P11	3	INCIDENT PRES ON THAWK LNCHR NO7	RAILING STB OF LCHR 7
P13	3	INCIDENT PRES ON HARPOON LNCHR NO3	RAILING AFT OF HCL NO3
P14	3	INCIDENT PRES ON MT23	RAILING AFT ON MT23
P17	3	REFLECTED PRES ON GSI	SURF MTD ON FRESNEL LENS
P18	3	REFLECTED PRES ON LNCHR NO7	SURF MTD LNCHR NO7
P19	3	REFLECTED PRES ON LNCHR NO7	SURF MTD LNCHR NO7
P23	3	REFLECTED PRES MT23	SURF MTD ON TRACK RADOME
S1	2	STRAIN RESPONSE OF MT21	FIRE CONTROL RADAR/ SERVO ASSEMBLY NEAR TRACK RADOM. CIR-CUMFERENTIAL DIR.
S2	2	STRAIN RESPONSE OF MT21	FIRE CONTROL RADAR/ SERVO ASSEMBLY NEAR TRACK RADOME. VERTICAL DIR.
S3	2	STRAIN RESPONSE OF MT21	FIRE CONTROL RADAR/ SERVO ASSEMBLY NEAR TRACK RADOME. OBLIQUE DIR. IN SURF.
S4	2	STRAIN RESPONSE OF SLQ-32	RADOME COVER LATCH MOUNTING FRAME. TRANSVERSE WRT BEAM
S5	2	STRAIN RESPONSE OF SLQ-32	RADOME COVER LATCH MOUNTING FRAME. VERTICAL (SPANWISE)
S6	2	STRAIN RESPONSE OF SLQ-32	RADOME COVER LATCH MOUNTING FRAME. OBLIQUE DIR.
T1	2,3	TIMING	TIME MARK GEN-ERATOR

18. NAVSTA TO ASSIST ONLOADING TEST EQUIP AT PIER.
BT
#5373

APPENDIX B

SLQ-32 NOTES

MAIN BATTERY FIRINGS IN USS NEW JERSEY

(BB-62)

29 APRIL 1984

Performed system diagnostic tests to baseline the system. Existing faults indicate a need for correlation adjustments in band 3, particularly chop and bit. There may be a leveling problem on the portside. Since all firing will be on the starboard side, the existing faults should not seriously affect testing.

This ship always operates with its enclosures stowed. They will be stowed through the test.

The ships crew reports that firing the forward mounts at angles less severe than those of this test will destroy enclosure door latches unless an inspection plate is removed from each enclosure. A plate will be removed from each enclosure during the test.

30 April 1984

Turret 2

Round 1 Injecting emitters in port and starboard. Emitters dropped out just before shooting so there was no ECM during the shot.

The shot had no visible effect.

Round 2 Injecting an emitter on the starboard side, engaging it with a combined ECM technique.

At the shot ECM stopped and stayed off.

High voltage power supply (HVPS) A10 lost high voltage, Memory Unit (RFMU) power switch/circuit breaker in the enclosure turned off.

Reset the HVPS, turned on RFMU system, ok.

Round 3 Inject and engage on starboard side.

At the shot ECM stopped and stayed off. Injected emitter dropped out, lost high voltage, system, reported appropriate faults, system reported starboard band 2 and 3 DFR faults.

Reseting program "SHIFT" brought the emitter back.

On the starboard forward transmitter door both gas springs popped loose on one end, the adjusting screw on the interlock switch was bent over.

The springs were removed, the screw bent back and the switch taped in, system functioning ok.

Round 4 Inject and engage on starboard side.

At the shot the ECM dropped out and returned in approximately 1/2 second. Upper latch on forward edge of the starboard forward radome door broken. Both latches on the port aft transmit door broken, opening port interlock.

Tied door closed with rope.

System functioning ok.

Round 5 Inject and engage on starboard side.

At the shot the ECM dropped out and returned. On the oscilloscope a momentary pulse was noted on the port side. SLA-10 blanker stopped working.

System functioning ok.

Round 6 Inject and engage on starboard side.

At the shot, ECM dropped out and returned latch on port aft radome door popped open.

Closed latch.

System functioning ok.

Round 7 Inject and engage on starboard side.

At the shot, ECM dropped out and return latch on port aft radome door popped open, RTV on starboard forward transmit radome being pushed in (RTV to fiberglass bond was poor to nonexistant prior to test).

SLA-10 working (card may have been jarred loose). Closed latch.

System functioning ok.

Round 8 Inject and engage on starboard side.

At the shot ECM dropped out, only the transponder returned.

RFMU switch went off, port aft radome door latch popped, blower switch off.

Turned switches on; although bouncing cables do not seem to be the problem, cables above the switches were tie-wrapped up and back.

Round 9 Inject and engage on starboard side.

At the shot the oscilloscope power plug was jarred loose. ECM was good when the scope was plugged in. Lower latch on starboard aft radome door popped open.

Closed latch.

System functioning ok.

Round 10 Inject and engage on starboard side.

At the shot ECM dropped out, transponder returned.

RFMU and blower switches off, latch on starboard aft radome door opened.

Turned on switches, closed latch.

System functioning ok.

Round 11 Inject and engage on port and starboard, no repeater on starboard.*

At shot starboard ECM dropped out and returned. Lost port high voltage, HVPS A10 lost high voltage.

RFMU switch went off, port aft transmitter door rope loosened opening interlock, HVPS A10 dead.

Turned on switch, tightened rope.

System functioning ok except for HVPS A10

Round 12 Injecting and engaging port and starboard, no repeater on starboard.

At the shot port and starboard ECM dropped out and returned.

System functioning ok except for HVPS A10.

* When injecting into port and starboard, if the emitters were engaged port then starboard there was no repeater on starboard, if engaged starboard then port engagement was ok. Further investigation is necessary.

After testing the system diagnostic tests were run to compare with the baseline. Except for problems directly related to HVPS A10, the system was essentially unchanged.

Round 13 Injecting and engaging port and starboard.

At the shot port ECM dropped out and returned, lost starboard high voltage, starboard forward transmit radome broken, top latch on starboard forward radome door broken opening interlock.

Taped radome, tied door.

System functioning ok except for HVPS A10, unknown effects of broken radome.

2 May 84

Turret 3

Round 19 Injecting and engaging port and starboard.

At the shot starboard ECM dropped out and in, port high voltage dropped

Closed interlock on port side (door with broken latches)

System functioning ok.

Round 20 Injecting and engaging port and starboard.

At the shot port and starboard ECM dropped out and in. Starboard forward transmit door latch opened.

Closed latch.

System functioning ok.

Round 21 Injecting and engaging port and starboard. Battle short on just before shot.

At shot ECM did not drop out. Removed battle short, lost port high voltage due to open interlock.

Closed interlock.

System functioning ok.

Round 22 Injecting and engaging on port and starboard sides.

At the shot port and starboard ECM dropped out and in.

System functioning ok.

Round 23 Injecting and engaging port and starboard sides.

At the shot port and starboard dropped out and in.

System functioning ok.

Round 24 Injecting and engaging port and starboard sides. Battle short on.

At shot ECM did not drop out. Removed battle short, lost port high voltage.

Closed interlock.

System functioning ok. Drop out during shots appears to be caused by interlocks opening and closing.

Round 25 Inject and engage on port and starboard sides.

At the shot starboard ECM dropped out and in, port dropped high voltage due to interlock.

Closed interlock.

System functioning ok.

TRIP REPORT

SUBJECT: Visit to USS NEW JERSEY (BB-62) 22 May 1984

ENCLOSURE: (1) Photographs of the Outboard Enclosures

1.0 BACKGROUND

1.1 The purpose of this visit was to assess gunblast damage to the SLQ-32. The New Jersey had reported several instances of latch failure during the firing of the 16 inch guns in training exercises. A set of spring latches modified with a 3/16" diameter travel limiting pin was sent to the ship as an interim fix. During a recent deployment over 200 16 inch rounds were fired. Prior to returning to Long Beach, the ship conducted a test firing with the main battery trained and elevated to create a high overpressure wave at the starboard enclosure.

1.2 Both enclosures exhibit similar damage characteristics, the starboard unit showed slightly greater stress. In general the gunblast damage is similar to but less than the damage sustained by the (V)3 enclosure in the direct course test.

2.0 OBSERVATIONS

2.1 The photographs in Enclosure (1) are arranged in port and starboard groups. The locations of detail photos are identified with arrows to areas on a central overview of the enclosure. In general polarizers and radomes in the aft quadrants were not deflected against their DF horns and show no damage. Semi-Omni Antennas were also undamaged.

2.2 On both port and starboard enclosures the inward deflection of the forward quadrant DFR doors deformed the semi rigid coax between the detectors and the beam forming lens of the Band 3 DFR's. The impact has marked the upper flange of the polarizers with footprints of the coax lines and has created a horizontal wrinkle in the inboard lamination of the polarizers (Photos P1 and S1). There are several faint striae in the inboard lamination (not visible in the photos) where the polarizer has struck the horn. The starboard unit has greater deformity and deeper markings than the port unit.

2.3 Band 2 polarizers are partially striated from the contact against their DFR's (Photos P2 and S2). There are more pronounced markings on the starboard unit.

2.4 The Transmitter Radome on the starboard forward quadrant was ruptured (Phote S26). Striae are visible across the entire inner face (Photo S2a) and a crack is visible in the lower inside edge.

Trip Report - USS NEW JERSEY (BB-62) - (Cont'd)

2.5 The plastic filler used where sections are joined (Top to side, Top and bottom of Transmitter - DFR door corner post) is cracked and separated. The starboard forward quadrant sustained the greatest separation, rivets are visibly stretched (Photo S3), the lower side has less separation (Photo S4), the aft DFR door opening shows the same stress (Photo S5). The port enclosure shows similar cracking (Photo P3) with little or no separation on the lower side of the corner post (Photo P4, P5, and P6).

2.6 Additional damage:

2.6.1 Adjustable DFR door positioner (Photos P1 and P2) is fractured.

2.6.2 The ship reports that the forward Quadrant Transmitter gas filled door positioners disconnected from the ball retainers during both the test firing and normal operations.

2.6.3 The RFMU circuit breaker in the power distribution box in the starboard enclosure kicks out during firing.

2.6.4 A number of door latches on each side have broken. The fault mode appears to be a fracture of the silbraze on the 3/16 limiting pin. The ship reports most latch failures occur on the transmitter doors. During deployment progressive cracking and latch failure was greatly reduced by opening the two 5 X 7 inspection plates on the inboard side of each enclosure during main battery firing. All inspection plates were in place during the test firing.

2.6.5 The interlock chain reportedly opened during firing. One transmitter door was tied shut with nylon line and could be pulled open about 1 1/2 inches.

3.0 OTHER FACTORS

3.1 The ship utilized the system in Stow. One enclosure has a servo amp problem. The NEW JERSEY does roll, even alongside the pier, although it takes about two minutes to cycle.

3.2 The inboard equipment sway braces are welded to the forward bulkhead neutral stringers. This is contrary to Grade A shock hardening methods.

3.3 The DCC sway braces are welded, at a 45 degree angle, to the overhead. This may be contrary to Grade A shock hardening methods.

Trip Report - USS NEW JERSEY (BB-62) - (Cont'd)

4.0 EVALUATION

4.1 As with the direct course test, a high intensity shock wave outboard will cause the 55 durometer door gasket to compress and flex the DFR door inward. Either or both conditions may allow the polarizer to strike the feed horns.

4.2 It would appear that the cause of enclosure structure separation and high outward stress on door latches are caused by a less than 15 PSI condition at the onside surfaces of the enclosure simultaneous to a normal 15.04 PSI internal pressure. Experiments with enclosure pressurization have shown that 3" H2O (0.12 PSI) above atmospheric is sufficient to bow the transmitter doors slightly outward. The ship's experience of fewer latch failures with a moderately free access between the inside and outside tends to support the pressure differential supposition.

4.3 As long as the upper sway braces are rigidly mounted to a shock receiving outboard bulkhead, the inboard equipment will take more punishment than is necessary.

5.0 RECOMMENDATIONS

5.1 Investigate the practicality of installing a combination template and travel limiting frame around the DFR and transmitter horns. If the point of contact is made on the inboard flange and in conjunction with the vertical sides of the polarizers, the polarizers could withstand considerable force.

5.2 During the forthcoming test firing of the IOWA, instrument one enclosure's transmitter doors to determine just how much pressure is applied to the enclosure and in what form and direction it is being applied.

5.3 Investigate the feasability of modifying the ball and socket arrangement of the gas filled door positioners to accept a locking screw similar to that which is used in racing car throttle linkages.

5.4 Suggest to NAVSEA that someone from the Battleship Design Group-Structural, at SUPSHIPS, Boston, visit NEW JERSEY prior to or during its forthcoming availability and make whatever sway brace recommendations they deem necessary.

5.5 It is recommended that during the 5 - 6 month availability the outboard enclosures be removed and restored to an RF1 condition. Elongated rivets should be removed and the enclosure drawn together before cosmetic filling is accomplished.

J. R. Lipman
Raytheon Service Company
C-3

APPENDIX D

EXPLANATION OF STRAINS MEASURED IN STBD SLQ-32

OUTBOARD DOOR RAIL

The blast wave advances over the equipment from the forward starboard corner of the antenna in a direction aft, up, and to port. The blast loads the radome enclosure and forward cover with the reflected overpressure measured by P5. Most P5s were in the range 8-9 psi. Incident overpressures were in the range 3 to 4 psi. This means the panel loads carried by the radome enclosure and the forward cover are in the range of 15,000 lbs to 25,000 lbs (estimated). The forward cover distributes this load by bearing on the door rails. The forces due to pressure are normal to the panels. Therefore, the panel loads are normal to the panels. The forward cover bears on a lip on the door rails. The radomes show imprints that perfectly match the receiver antennae feed horns. This indicates that the blast wave is pushing the radomes onto the antennae. When this occurs the blast load on the radome cover is carried by the antennae feed horns, which in turn transfer the load to the primary internal structure of the antenna which consists of large castings and machined elements. Some of the load, but not all of it, is carried by the circumferential framework which supports the latches. Strain S4 is believed largest because it measures the strain due to the blast load on the forward cover being reacted by the lip of latch frame. S5 is slightly in compression (-300m strain). There may be combined axial loading of the beam which offsets some extension of longitudinal fibers due to bending at the gauge location. Calculations show S4 and S5 are nearly principal directions and carry 21,100 and 4,900 psi respectively. Since it is very unlikely that the instruments were at the points of maximum stress in the material, the system is probably right on the verge of serious failures at these blast pressure levels. Blast hardening could be accomplished by creating additional load paths to the primary structure. These could be pads on the enclosure covers that bear on reinforced points connected to the primary internal structure.

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